1 Review of Pre-requisites

Analysis of any transistor amplifier circuit proceeds with the following steps:

- DC analysis: Open all capacitors short all inductors and calculate DC parameters of interest such as I_C, I_D and $V_{GS} - V_T$. This should enable you to find the parameters of small signal analysis such as g_m, r_π and r_o.
- AC analysis has the following steps:
  1. Step 1: Short all DC voltage sources and open all DC current sources.
  2. Step 2: Short all capacitors and open all inductors.
  3. Step 3: Replace the transistor with its own small signal equivalent.

In doing all the steps see if you can bring any simplification.

1.1 Problems for Practice

1. The MOSFET in Fig.(1) has $V_T = 0.7V$, and $\mu_n C_{ox} = 500\mu AV^2$. The drain current in the device is 1mA. Find $\frac{W}{L}$ of the device and the small signal gain v_i to v_o. Assume that the capacitors are infinite.

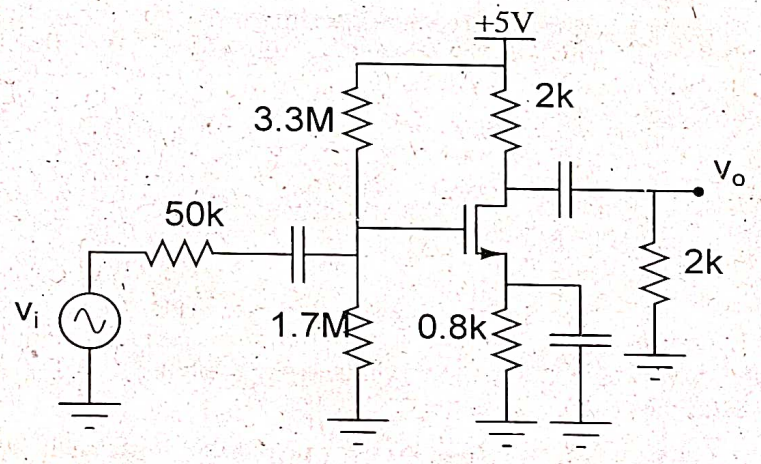

Figure 1: Problem 1

Lets first do the DC analysis. The dc equivalent circuit is shown in Fig.(2):

Since MOSFET gate does not allow any current, we can use voltage divider equation to find V_G:

$$g_m = \frac{2I_D}{V_{GS} - V_{Tn}} = \frac{2 \times K_n (V_{GS} - V_{Tn})^2}{V_{GS} - V_{Tn}} = 2K_n(V_{GS} - V_{Tn})$$

$$= 2\sqrt{I_D K_n}$$

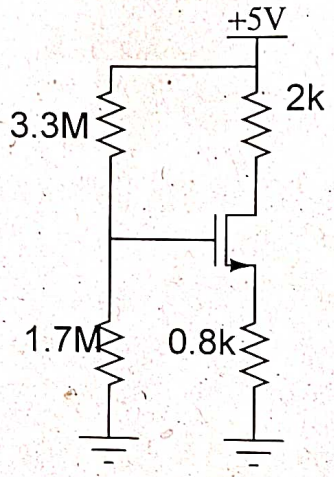

Figure 2: DC equivalent for Problem 1

$$V_G = \frac{1.7M}{3.3M + 1.7M} \times 5 = 1.7\text{V}$$

Since the source current is also the drain current, we have $I_S = I_D = 1mA$ from which we have $V_S = 0.8V$. Now, $V_{GS} = V_G - V_S = 0.9V$. The transconductance of the MOSFET:

$$\begin{aligned} g_m &= \frac{2I_D}{V_{GS} - V_T} && (1) \\ &= \frac{2 \times 1 \times 10^{-3}}{0.2} && (2) \\ &= 10mS && (3) \end{aligned}$$

By applying the steps sequentially, we obtain the small signal equivalent of the amplifier. See Fig.(3) shows the amplifier after applying step 1, that is shorting the 5V DC source.

We notice that 1.7M and 3.3M coming in parallel with each other. As the second step indicates we short the capacitors in the circuit resulting in Fig.(4).

It is easy to see that the source is connected to ground and the drain and load resistors come in parallel. Fig.(5) shows the final small signal circuit, from which the gain can be computed.

We have,

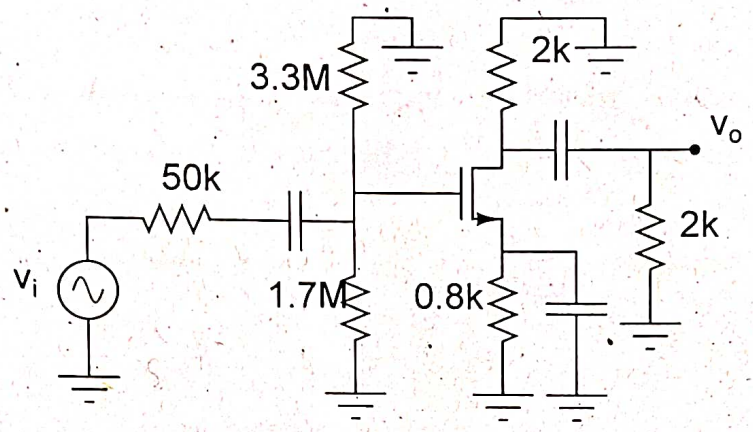

Figure 3: Step 1 of AC analysis

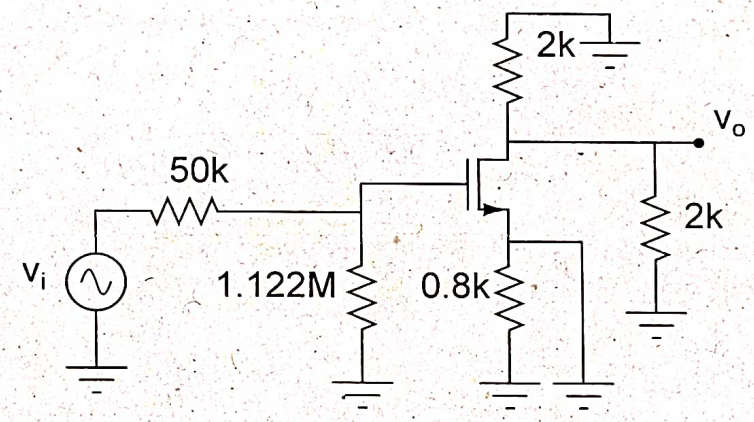

Figure 4: Step 2 of AC analysis

$$
\begin{aligned}
v_{gs} &= \frac{3.3M \parallel 1.7M}{50K + 3.3M \parallel 1.7M} v_i && (4)\\
&= 0.957 v_i && (5)\\
v_o &= -g_m v_{gs} \times 1k && (6)\\
&= -9.57. && (7)
\end{aligned}
$$

To find the aspect ratio we use the basic formula for I_D, which is

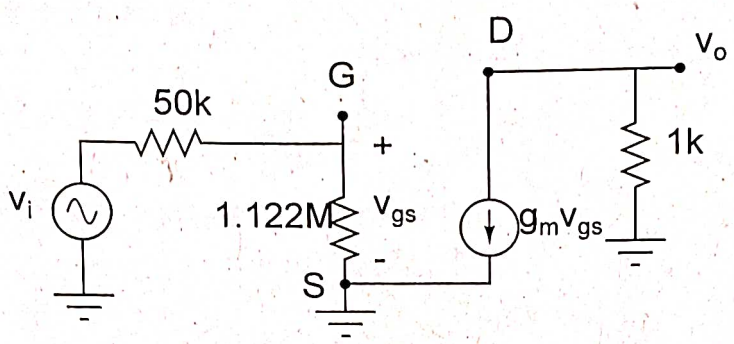

Figure 5: Final incremental circuit

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2 \tag{8}$$

$$\Rightarrow \frac{W}{L} = \frac{2I_D}{\mu_n C_{ox}(V_{GS}-V_T)^2} = 100. \tag{9}$$

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1 Review of Pre-requisites-2

Analysis of any transistor amplifier circuit proceeds with the following steps:

- DC analysis: Open all capacitors, short all inductors and calculate DC parameters of interest such as I_C, I_D and $V_{GS} - V_T$. The ac voltage source must be short circuited and ac current sources must be open circuited. Assertain that the circuit is operating in forward active mode for BJT and saturation region for MOSFET. This should enable you to find the parameters of small signal analysis such as g_m, r_π and r_o.
- AC analysis has the following steps:
  1. Step 1: Short all DC voltage sources and open all DC current sources.
  2. Step 2: Short all capacitors and open all inductors.
  3. Step 3: Replace the transistor with its own small signal equivalent.

In doing all the steps see if you can bring any simplification.

1.1 Solved Problems

1. Determine the small-signal voltage gain of a common-source circuit containing a source resistor shown in Fig.(1). The transistor parameters are $V_{TN} = 0.8$V, $K_n = 1mAV^2$ and $\lambda = 0$. Assume that the capacitors are infinite.

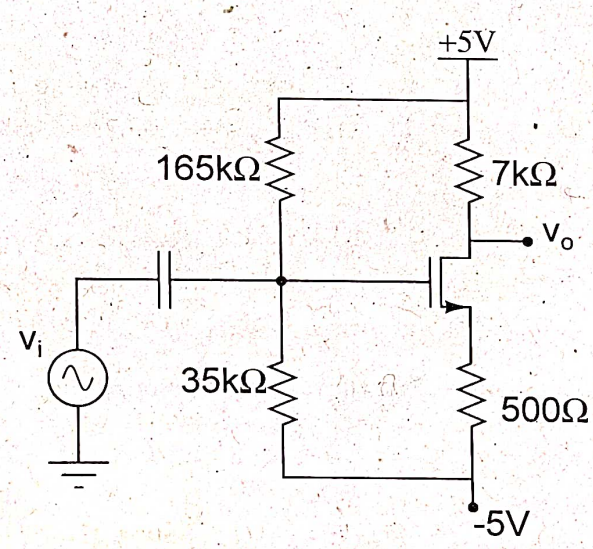

Figure 1: Problem 1

The DC equivalent circuit is shown in Fig.(2). This figure is arrived based on potential divider rule which states that,

$$V_G = \frac{V_{DD}R_2 + V_{SS}R_1}{R_1 + R_2} \quad (1)$$

$$= \frac{5 \times 35 - 5 \times 165}{165 + 35} = -3.25 \quad (2)$$

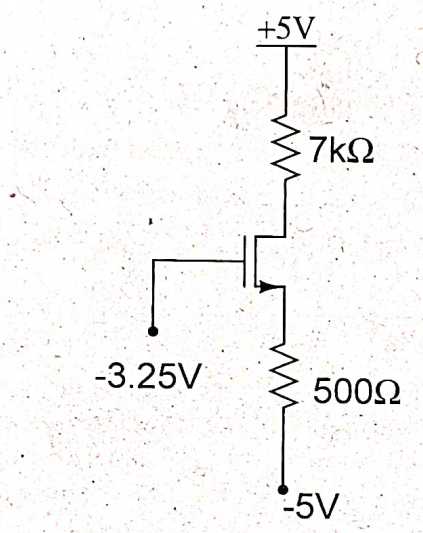

Figure 2: Problem 1:DC equivalent circuit

Applying KVL around the gate source loop, we get:

$$V_G = V_{GS} + I_D R_S + V_{SS} \quad (3)$$

$$= V_{GS} + K_n R_S (V_{GS} - V_T)^2 + V_{SS} \quad (4)$$

$$-3.25 = V_{GS} + 0.5(V_{GS} - 0.8)^2 - 5 \quad (5)$$

Where we have assumed that the transistor is operating in saturation region. This has to be confirmed at some stage. Now, the above equation transforms to a quadratic equation:

$$0.5V_{GS}^2 + 0.2V_{GS} - 1.43 = 0 \quad (6)$$

Eq.(6) has two solutions namely $V_{GS1} = 1.503$V and $V_{GS2} = -1.903$V. We discard the second solution as $V_{GS2} < V_T$, implying that the device is in off condition which is false. The drain current is:

$$I_D = K_n(V_{GS} - V_T)^2 = 0.494mA \approx 0.5mA \tag{7}$$

Applying KVL over the drain source loop, we obtain the $V_{DS} = 6.25$V. Now, we can see that $V_{DS} \geq V_{GS} - V_T$, asserting that the device is in saturation region. The transconductance of the MOSFET is $g_m = 2K_n(V_{GS} - V_T) = 1.4m$S and $r_o = \infty$ as $\lambda = 0$. Having obtained these parameters, we obtain the small signal model using the steps outlined above. After applying the step 1, the circuit appears as shown in Fig.(3).

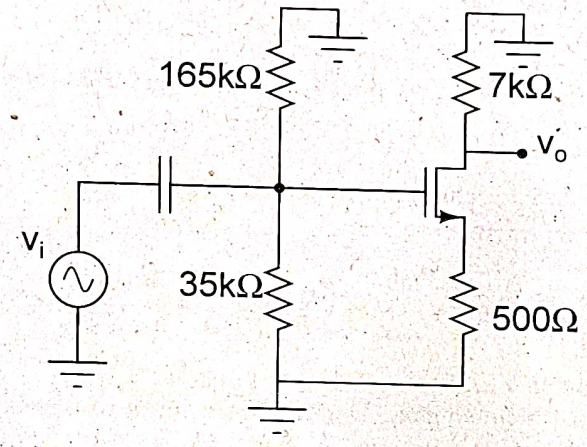

Figure 3: Problem 1: Step 1

We can see that $165k\Omega$ and $35k\Omega$ can be combined in parallel. After applying the second step and third step we obtain the circuit in Fig.(4).

The output voltage is,

$$v_o = -g_m v_{gs} R_D = -1.4 \times 7 v_{gs} \tag{8}$$

We also have,

$$\begin{aligned} v_i &= v_{gs} + v_s && (9)\\ &= v_{gs} + g_m R_S v_{gs} && (10)\\ &= v_{gs}(1 + g_m R_S) && (11)\\ \Rightarrow v_{gs} &= \frac{v_i}{1 + g_m R_S} && (12) \end{aligned}$$

The small signal voltage gain is,

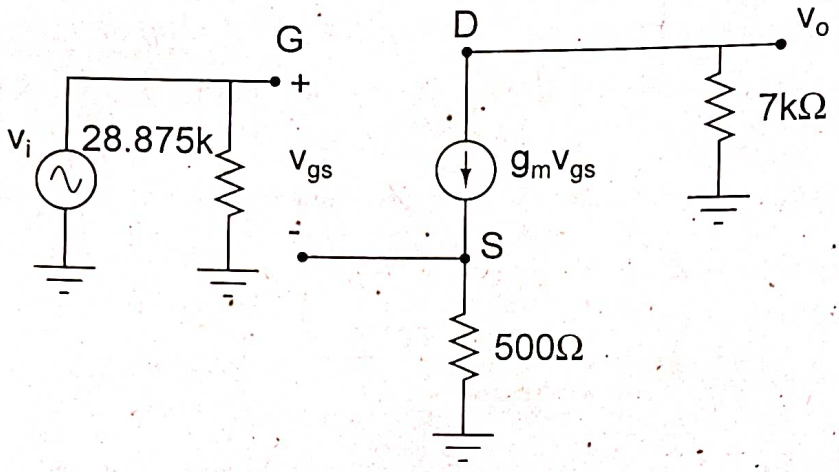

Figure 4: Problem 1: After step 3

$$A_V = \frac{v_o}{v_i} = -\frac{g_m R_D}{1 + g_m R_S} = -\frac{1.4 \times 7}{1 + 1.4 \times 0.5} = -5.76 \tag{13}$$

2. For the circuit in Fig.(5), let $\beta = 100$, $V_{BE(on)}0.7$V and $V_A = 100$V. Determine the small-signal voltage gain. Determine the input resistance seen by the signal source and the output resistance looking back into the output terminal. Assume that the capacitors are infinite.

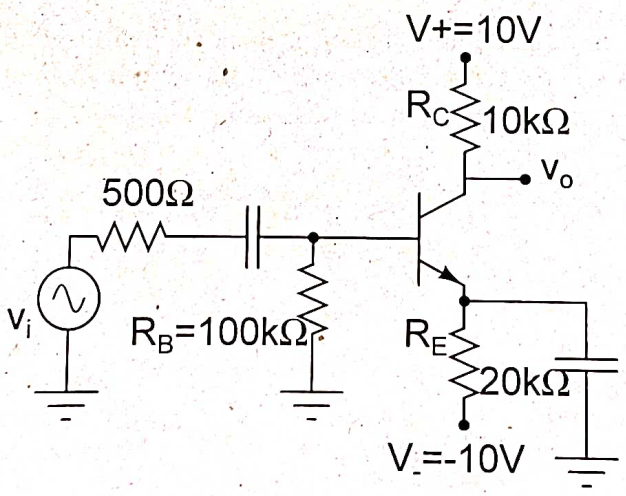

Figure 5: Problem 2

Treating the capacitors as open circuit, the DC equivalent will contain the reistors R_B, R_C and R_E. Applying KVL around the base-emitter loop, we get:

$$
\begin{aligned}
0 &= I_B R_B + V_{BE(on)} + I_E R_R + V_{EE} && (14)\\
0 &= I_B R_B + (1+\beta) I_B R_E + V_{EE} + V_{BE(on)} && (15)\\
\Rightarrow I_B &= -\frac{V_{EE} + V_{BE(on)}}{R_B + (1+\beta) R_E} && (16)\\
I_B &= -\frac{-10 + 0.7}{100k + (1+100)20k} = 4.387\mu\text{A} && (17)
\end{aligned}
$$

Now, $g_m = \frac{\beta I_b}{V_T h} = 16.873m\text{S}$, $r_\pi = \frac{\beta}{g_m} = 5.927k\Omega$ and $r_o = \frac{V_A}{I_C} = 228k\Omega$. Proceeding sequentially through all the steps we arrive at the small signal model shown in Fig.(6). For the incremental gain we follow through the calculations given under:

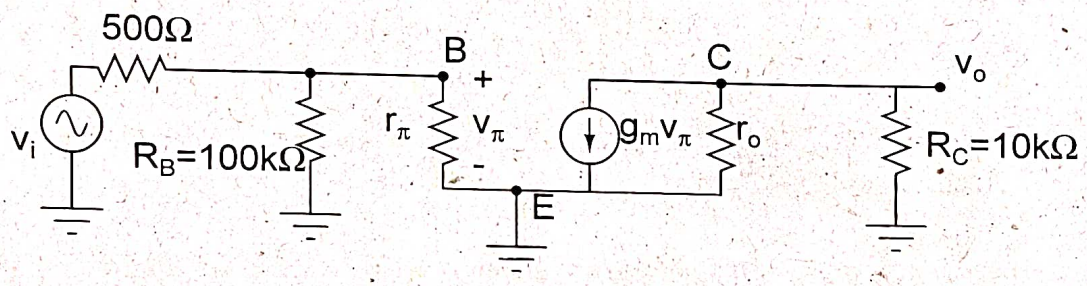

Figure 6: Problem 2: Small signal circuit

$$
\begin{aligned}
v_o &= -g_m (R_C \parallel r_o) v_\pi && (18)\\
v_\pi &= \frac{R_B \parallel r_\pi}{500 + R_B \parallel r_\pi} v_i && (19)\\
\Rightarrow A_v &= \frac{v_o}{v_i} = -g_m (R_C \parallel r_o) \frac{R_B \parallel r_\pi}{500 + R_B \parallel r_\pi} && (20)\\
&= -148VV. && (21)
\end{aligned}
$$

The input impedance is $R_i = 500 + 100k \parallel r_\pi = 6.09k\Omega$ and the output resistance is $R_o = R_c \parallel r_o = 9.58k\Omega$. Note in calculating the output impedance we must find the Thevinin resistance looking from the output terminals.

3. Determine the small-signal voltage gain of a circuit (shown in Fig.(7)) biased with a constant-current source and incorporating s source bypass capacitor. The transistor parameters are: $V_T = 0.8\text{V}$, $K_n = 1mAV^2$ and $\lambda = 0$. Assume that the capacitors are infinite.

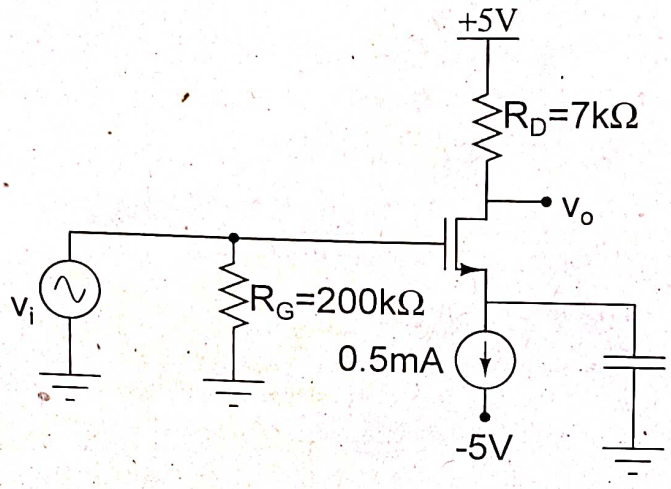

Figure 7: Problem 3

Let us assume that the transistor is biased in saturation region and hence by definition:

$$I_D = K_n(V_{GS} - V_T)^2 \tag{22}$$

$$\Rightarrow V_{GS} = \sqrt{\frac{I_D}{K_n}} + V_T = 1.507V \tag{23}$$

We still need to assert that the transistor is operating in saturation region, to that end we draw the DC equivalent circuit shown in Fig.(8).

Note that in the DC equivalent circuit the ac signal source must be grounded, if it were an ac current source it should have been open circuited. The terminal voltages can be obtained by applying KVL around their respective loops:

$$V_D = V_{DD} - I_D R_D = 5 - 7 \times 0.5 = 1.5 \tag{24}$$

$$V_{GS} = V_G - V_S = -V_S = 1.507V \tag{25}$$

$$\Rightarrow V_S = -1.507V \tag{26}$$

$$V_{DS} = V_D - V_S = 3.007V. \tag{27}$$

We notice that the condition for saturation $V_{DS} \geq V_{GS} - V_T$ is satisfied. The small signal equivalent circuit can be deduced from the sequence of steps and is shown in Fig.(9). The transconductance is $g_m = 2\sqrt{K_n I_D} = 1.414mS$.

We notice that $v_{gs} = v_i$ and $v_o = -g_m v_{gs} R_D$ and hence the gain is,

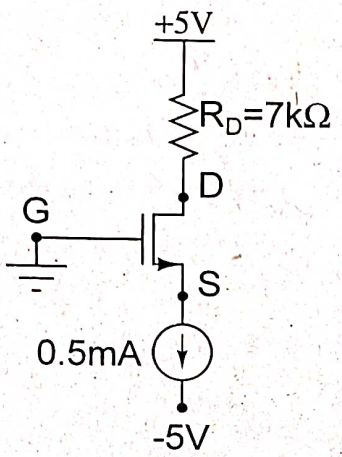

Figure 8: Problem 3: DC equivalent circuit

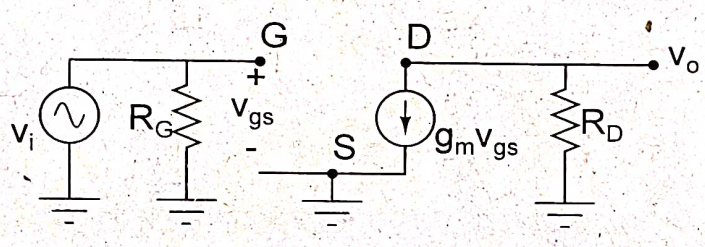

Figure 9: Problem 3:AC equivalent circuit

$$A_v = \frac{v_o}{v_i} = -g_m R_D = -1.414 \times 7 = -9.9 \tag{28}$$