VIT
Vellore Institute of Technology

School of Information Technology and Engineering

Fall Semester 2023-2024

Continuous Assessment Test – II

Programme Name & Branch : B.Tech-IT

Course Name & Code: BITE301L – Computer Architecture and Organization

Class Number (s): VL2023240100171, VL2023240100172

Slot: B1+TB1, B2+TB2

Faculty Names: Prof. Asha M M & Prof.Nagarajan B

Exam Duration: 90 Min. **Maximum Marks: 50**

General Instruction(s):

Answer ALL Questions (5 * 10 = 50 Marks)

1. A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 4800 characters per second. The CPU is fetching and executing instructions at an average rate of one million instructions per second.

   a) By how much will the CPU be slowed down because of the DMA transfer? (6 Marks)

   b) How much more percent the CPU slows down when 16 –bits words are transferred to memory using cycle stealing? (4 Marks)

2. Design a RAM memory to find how many 256x8 RAM chips are needed to provide a memorycapacity of 4096 bytes.
   i. How many bits will each memory address contain? 8
   ii. Find the total number of chips 16
   iii. How many address lines must go to eachchip? 12 & 8
   iv. How many lines must be decoded for the chip select inputs? Specify the size of the decoder. 4 x 16
   v. With the neat sketch show result of internal memory organization.

3. Assume 8-bit 2's complement numberrepresentation, multiply the multiplicand A= 11001101 by the multiplier B=10110010 using both Booth algorithm and the bit-pair recoding Booth algorithm.

4. Apply the division algorithm restoring and non-restoring, perform the unsigned binary division for the decimal operands 132 and 25. Assume appropriateregister sizes for the given operands. Show the application of the algorithmic steps over the numbers in a table with the flowchart. Convert the result in binary to decimal form.

5. Consider the decimal real numbers 12.03125 and 9.25.
   a) Convert to binary form and represent in IEEE 754 single precision and double precision format. (4 Marks)
   b) Perform the floating point addition using the algorithm step by step. (3 Marks)
   c) Perform the floating point subtraction using the algorithm step by step. (3 Marks)