REG.NO.:

SJM 323

VIT

Vellore Institute of Technology

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING

CONTINUOUS ASSESSMENT TEST - II

FALL SEMESTER 2024-2025

SLOT: B2 + TB2

Programme Name & Branch	**: B.Tech CSE**
Course Code and Course Name	**: BCSE303L Operating Systems**
Faculty Name(s)	**: N.Narayanan Prasanth (Common to all faculties)**
Class Number(s)	**: Common to all classes**
Date of Examination	**: 14-10-2024**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

Answer All Questions

M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes

CO2: Design scheduling algorithms to compute and compare various scheduling criteria.

CO3: Apply and analyze communication between inter process and synchronization techniques.

CO4: Implement page replacement algorithms, memory management problems and segmentation.

<table>
<tr><th>Q. No</th><th>Question</th><th>M</th><th>CO</th><th>BL</th></tr>
<tr><td>1.</td><td>Consider the following snapshot of a system:
<table>
<tr><th rowspan="2">Process</th><th colspan="4">Allocation</th><th colspan="4">Max</th><th colspan="4">Available</th></tr>
<tr><th>A</th><th>B</th><th>C</th><th>D</th><th>A</th><th>B</th><th>C</th><th>D</th><th>A</th><th>B</th><th>C</th><th>D</th></tr>
<tr><td>P_0</td><td>6</td><td>0</td><td>1</td><td>2</td><td>4</td><td>0</td><td>0</td><td>1</td><td>3</td><td>2</td><td>1</td><td>1</td></tr>
<tr><td>P_1</td><td>2</td><td>7</td><td>5</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="4" rowspan="4"></td></tr>
<tr><td>P_2</td><td>2</td><td>3</td><td>5</td><td>6</td><td>1</td><td>2</td><td>5</td><td>4</td></tr>
<tr><td>P_3</td><td>1</td><td>6</td><td>5</td><td>3</td><td>0</td><td>6</td><td>3</td><td>3</td></tr>
<tr><td>P_4</td><td>1</td><td>6</td><td>5</td><td>6</td><td>0</td><td>2</td><td>1</td><td>2</td></tr>
</table>
Using the banker's algorithm,
1. Calculate the Resource Need of every Process. (2)
2. Check if the system is in safe state? If it is, find the safe sequence. (5)
3. If a request from P3 arrives for (2,1,0,0), can the request be granted immediately? Explain. (3)</td><td>10</td><td>02</td><td>3</td></tr>
<tr><td>2.</td><td>a) In a modern multi-robot warehouse, robots perform tasks like retrieving items from storage, transporting them to packing areas, and restocking items. These robots often need to access shared storage shelves. To avoid collisions and ensure that only one robot accesses storage aisle at a time, synchronization is needed. Show how Bakery algorithm can be used to ensure safe, fair, and efficient coordination among robots competing for shared resources. Discuss your answer with a neat pseudo code.</td><td>7</td><td>03</td><td>6</td></tr>
<tr><td></td><td>b) Show how does the signal() operation associated with monitors differ from the corresponding operation defined for Semaphores?</td><td>3</td><td></td><td></td></tr>
</table>

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3.	Multiple clients can request connections to the database server; however, only 10 connections can be handled by the server at a time. Recommend a suitable synchronization mechanism to manage the given scenario, so as to avoid race condition and ensure proper resource management. The synchronization mechanism should provide flexible resource allocation, allowing multiple clients to coordinate their access effectively. What would happen if more than 10 clients attempt to connect simultaneously? Justify the selection of synchronisation mechanism with a neat pseudo code. Discuss its pros and cons in view of the scenario.	10	03	6
4.	a) Given memory partitions of 100K, 500K, 200K, 300K, and 600K (in order), how would each of the First-fit, Best-fit, and Worst-fit algorithms place processes of 212K, 417K, 112K, and 426K (in order)? Which algorithm makes the most efficient use of memory?	6	04	3
	b) Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, then compute the effective memory access time.	4		
5.	Consider the following Page Reference String: d, c, b, a, d, c, e, d, c, b, a, e. 1. Calculate the number of page faults using FIFO that would occur if the number of frames is 3 and 4 respectively. "Should the increase in number of frames (i.e. 3 to 4), increase the number of page faults?" – Comment on the statement for the given scenario. (5) 2. Calculate the number of page faults, hit ratio and fault ratio using LRU that would occur if the number of frames is 3. (5)	10	04	3

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