



VIT

Vellore Institute of Technology
(Accredited to be University under section 3 of UGC Act 1956)

REG.NO.: UBCT0108

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

SLOT: **F1+TF1**

Programme Name & Branch : BTech ECE/CSE
 Course Code and Course Name : BECE102L & Digital System Design
 Faculty Name(s) : PRAYLINE RAJABAI C, ANTONY XAVIER GLITTAS X, SUMIT KUMAR JINDAL, HEMALATHA K, ANAND S, AVINASH CHANDRA, RAGUNATH G, ARUN DEV DHAR DWIVEDI, NAVEEN MISHRA, NIROJ KUMAR SAHU, SHANIDUL HOQUE, MOHIUL ISLAM, LAVANYA N, GEORGE JACOB, HEMANTA KUMAR SAHU, KALYANBRATA GHOSH, VIVEK RAJPOOT, SHILPI RUCHI KERKETTA, SUKANTA KUMAR TULO, ABHISHEK NARAYAN TRIPATHI, RAJESHKUMAR V, SUMATHI G, DILIP KUMAR CHOUDHARY, TANMAYA KUMAR DAS, MANGAIYARKARASI R, ROHIT MATHUR, RAHUL MANOHAR O

Class Number(s) : VL2025260102573, 2579, 3578, 3580, 3583, 3585, 3587, 3589, 3591, 3593, 3598, 3600, 3603, 3605, 3608, 3610, 3613, 3619,3622,3627,3630,3634,3643,3645,3647,3651,3657

Date of Examination : 22.08.25
 Exam Duration : 90 minutes (9.30 AM – 11.00 AM) Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level
(1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes are:

C01: Optimize the logic functions using and Boolean principles and K-map. ✓
 C02: Model the Combinational and Sequential logic circuits using Verilog HDL.
 C03: Design the various combinational logic circuits and data path circuits.

S.No.	Question	CO	BL	Marks
1.	Use Boolean law/postulates to derive the minimized expression for the function $F = (B' + C)(B' + C')(A + B + C'D)$ Also, determine the dual and complement expression of the minimized function.	1	BL3	5+5
2.	Apply the K-Map on the Boolean function $F(A, B, C, D) = \sum m(0, 3, 7, 6, 8, 13, 14) + \sum d(2, 4, 10)$ to obtain the minimized SOP and POS and also draw the logic diagram for the minimized SOP with NOR gates only.	1	BL3	10



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3.	<p>(a) Draw the logic diagram for verilog code given below:</p> <pre> module Circuit_B (F1, F2, F3, A0, A1, B0, B1); output F1, F2, F3; input A0, A1, B0, B1; nor (F1, F2, F3); or (F2, w1, w2, w3); and (F3, w4, w5); and (w1, w6, B1); or (w2, w6, w7, B0); and (w3, w7, B0, B1); not (w6, A1); not (w7, A0); xor (w4, A1, B1); xnor (w5, A0, B0); endmodule </pre> <p>b) Recognize the output of the each operations in the verilog code. Consider the inputs are binary numbers.</p> <ol style="list-style-type: none"> 10111 && 1110 1100 ^1010 1 1 x 0 1 1010 % 100 1100 (~(101)) 	2	BL2	5+5
4.	<p>Develop a dataflow modeling verilog code for the design below.</p> <pre> module Circuit_A (A, B, C, D, F); input A, B, C, D; output F; wire w, x, y, z, a, d; not (a, A); not (d, D); or (y, a, C); and (x, B, C, d); or (z, y, A); and (w, z, B); and (F, x, w); endmodule </pre>	2	BL3	10
5.	<p>Construct a combinational circuit which has three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the output is the one's complement of input.</p>	3	BL3	10