T/E/TX

Reg. No: 23BBS0025

Final Assessment Test – May 2024

Vellore Institute of Technology

Course: **CBS1004 - Computer Architecture and Organization**

Class NBR(s): **3602/3603** Slot: **F2**

Time: **Three Hours** Max. Marks: **100**

- **KEEPING MOBILE PHONE/ELECTRONIC DEVICES EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

Answer any TEN Questions

(10 X 10 = 100 Marks)

1. Explain in detail the different types of Addressing modes with examples.

2. a) The 8-bit registers AR, BR, CR, and DR initially have the following values: AR 11110010, BR 11111111, CR 101 11001, and DR 11101010. Determine the 8-bit values in each register after executing the following sequence of micro-operations. **[5]**

   AR <- AR + BR Add BR to AR
   CR <- CR ∧ DR, BR <- BR + 1 AND DR to CR, increment BR
   AR <-AR - CR Subtract CR from AR.

   b) Draw the flowchart for the implementation of addition and subtraction of two signed magnitude numbers 'A and B' **[5]**

3. a) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: An operation code, a registered code part to specify one of 64 registers, and an address part. **[5]**

   i. How many bits are there in the operation code, the register code part, and the address part?
   ii. Draw the instruction word format and indicate the number of bits in each part.
   iii. Specify the address range and no of bits used for address bits.

   b) Explain with a neat diagram five stage instruction cycle. **[5]**

4. A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks, each containing 256 eight-bit words.

   How many bits are required for addressing the main memory?

   How many bits are needed to represent the TAG, SET and WORD fields? Draw the diagram for cache Hit and Miss.

5. a) A DMA controller transfers 32-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. Each character is 8 bits long. The CPU fetches and executes instructions at an average rate of 1 million per second. How much will the CPU be slowed down because of the DMA transfer? **[6]**

   b) What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each? **[4]**

6. Describe the usage of RAID architecture in external storage systems with a diagram.

7. Perform the division of the following numbers using the non-restoring division algorithm. Dividend (Q) = 9, Divisor (B) = 5. Represent the flowchart of the same.

8. a) A 400 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle count: [6]

Instruction Type	Instruction Count	Clock Cycle Count
Integer arithmetic	450000	1
Data transfer	320000	2
Floating point	150000	2
Control transfer	80000	2

Determine the effective CPI, MIPS rate, and execution time (T) for this program.

b) We want to speed up computer performance with an additional unit for calculating in floating-point format. This unit is 20 times faster than the same operations without a unit. What percentage of total computer time must this unit be active to increase computer speed by 2.5 times? [4]

9. Solve (-9) × (13) in sequence of steps using a booth algorithm with the necessary flow chart representation.

10. Describe the working model of multi-core architecture using threading with a neat diagram.

11. a) List out various Block replacement algorithms used in cache memory with example. [4]

b) A computer system employs a write-back cache with a 90% hit ratio for writes. The cache operates in "Look Aside" and has a 80% read hit ratio. Reads account for 60% of all memory references and writes account for 40%. If the main memory cycle time is 300ns and the cache access time is 30ns, what would be the average access time for all references (reads as well as writes)? [6]

12. a) Explain in detail about instructional pipelining with example. [6]

b) How do you establish communication between an I/O device and processor? What is the role handshaking technics in this process? [4]

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