VIT
Vellore Institute of Technology

School of Computer Science and Engineering

FALL SEMESTER 2024-2025

CAT-1

Date: 29.8.24

Slot: E1

Programme Name & Branch: B.Tech -CSE

Course Name & Code: BECE102L & Digital Systems Design

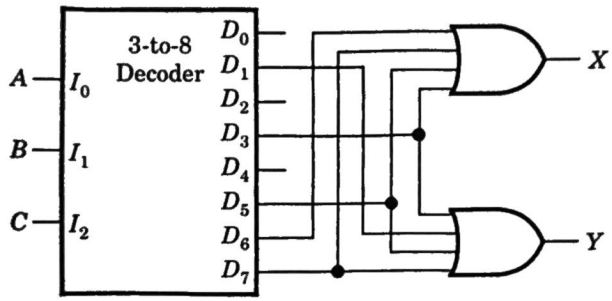
Faculty Name (s): Anitha R, Lavanya N, Palla Penchalaiah, Avinash Chandra, Rajesh N, Shweta B Thomas, Saurabh Nagar, Anju Thomas, Sidharth Gautam, Jaffino, Hemanta Kumar Sahu, Anand S, Nawaz Shafi, Vetriveeran Rajamani, Hemalatha K, Sukanta Kumar Tulo, Raja Sellappan, Niroj Kumar Sahu, Mangaiyarkarasi R

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s): 1. Answer ALL

Q. No	Question	Marks	CO	BL
1.	Implement the following Boolean function F, together with the don't-care conditions d, draw the circuit using only two input NAND gates: F(A, B, C, D) = Σ m (0, 1, 2, 6,7, 8, 9, 10) + Σ d (3, 11,15)	10	1	BL3
2.	Simplify the following Boolean function "F" by Boolean laws/postulates/theorems (k – Maps are not allowed). Draw the circuit diagram (a) $F(A,B,C) = \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$ (b) $F(A,B,C) = (A+\bar{B}+\bar{C})(A+\bar{B}+C)(A+B+\bar{C})$	10	1	BL3

3.	Draw the circuit diagram for the Verilog code given below. Convert the circuit using Basic gates.
	module cat3(a,b,c,d,f);
	input a,b,c,d;
	output f;
	wire w1,w2,w3,w4;
	nand g1(w1,a,c);
	nand g2(w2,b,b);
	nand g3(w3,w2,c);
	nand g4(w4,b,d);
	nand g5(f,w1,w2,w4);
	endmodule
		10	2	BL2

4.	Design a combinational logic circuit which has 4 bit BCD as an input (PQRS) and two outputs Y and Z. The output Z = 1, whenever there is an even number of 1's present in the input number. The Y = 1, whenever there is a prime number as input (consider 0 and 1 as prime number). Write the dataflow Verilog HDL.	10	3	BL3
5.	Design the logic circuit using 4:1 MUX to implement each function X and Y represented in terms of a 3-to-8 decoder by using following specifications: i). Use A and C as select lines for the 4:1 MUX implementing function X. ii). Use A and B as select lines for the 4:1 MUX implementing function Y. 	10	3	BL3