REG.NO.:

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT: C1 + TC1

Programme Name & Branch : B. Tech Computer Science and Engineering
Course Code and Course Name : BCSE205L and Computer Architecture and Organization
Faculty Name(s) : Common to all
Class Number(s) : VL2024250501363, VL2024250501365, VL2024250501379, VL2024250501382, VL2024250501386, VL2024250501389, VL2024250501393, VL2024250501395, VL2024250501403, VL2024250501417, VL2024250501419, VL2024250501421, VL2024250501423, VL2024250501425, VL2024250501427, VL2024250501431, VL2024250501435, VL2024250501441, VL2024250501445, VL2024250501449, VL2024250501454, VL2024250501476

Date of Examination : 18-03-2025
Exam Duration : 90 minutes
Maximum Marks: 50

General instruction(s):

- Answer All Questions
- CO1-Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating-point arithmetic operations.
- CO2- Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyse and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
- CO3-Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

<table>
<tr><th>Q. No</th><th>Question</th><th>M</th><th>CO</th><th>BL</th></tr>
<tr><td>1.</td><td>a) Computer A runs a program in 40 seconds with a 2 GHz clock. Computer B is designed to run the same program in 20 seconds but requires twice the clock cycles of Computer A. Analyse how the relationship between execution time, clock cycles, and clock rate influences the performance of Computer B compared to Computer A. Discuss the trade-offs involved in increasing clock rates versus the number of clock cycles required.</td><td>5</td><td>CO1</td><td>BL4</td></tr>
<tr><td></td><td>b) As part of enhancing the functionality of an architecture, it is necessary to incorporate a complex instruction into its instruction set. Considering the trade-offs involved, analyse whether a hardwired or microprogrammed control approach is more suitable for implementing this update. Provide a detailed justification for your recommendation, supported by an explanatory diagram.</td><td>5</td><td></td><td></td></tr>
<tr><td>2.</td><td>Evaluate the given expression A = (B + C) * (D - E) and compute the memory to encode, memory to store, memory traffic for 3, 2, 1, and 0 address machines. Assume the following: Addresses are 24 bits, Data values are 24 bits, Opcodes are 8 bits, and Word length is 8 bits.
Note: Specify the answer in this format.
<table>
<tr><th>1</th><th>Memory to store</th><th>Memory to Encode</th><th>Memory to Fetch</th><th>Memory to Execute</th><th>Memory Traffic</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table></td><td>10</td><td>CO1</td><td>BL3</td></tr>
<tr><td>3.</td><td>a) Consider a machine with a byte addressable main memory of 2^20 bytes and block size of 8 bytes. Assume that a direct mapped cache</td><td>4</td><td>CO2</td><td>BL4</td></tr>
</table>

	consisting of 32 lines is used with this machine. i) How is a 20-bit memory address divided into tag, line number, and byte number? ii) Into what line would bytes with each of the following addresses be stored? 1) 1101 0000 0001 1101 0001 2) 1010 1010 1010 1010 0010			
	b) Draw the circuit for ROM memory which can hold $2x2^{10}$ words with word size 64 using an integrated chip of 2^{10} words with word size of 32. Give the range of addresses for each of the ICs in the circuit.	6		
4.	a) Using a diagram, demonstrate how direct mapping organizes and stores the given sequence of memory blocks in a cache. Assume that 4-line cache memory is used.(Use the same sequence in part b)	3	CO2	BL3
	b) Apply the block replacement algorithm (FIFO and Optimal) on the sequence of block references provided, considering a fully associative cache of size 128 B with block size 32 bytes. The sequence is as follows: 5, 7, 7, 4, 1, 5, 0, 7, 7, 0, 13, 6, 5, 1, 12, 5 Summarize the detail Algorithm | FIFO | Optimal Number of hits Number of misses Total number of references Hit Ratio Miss Ratio	7		
5.	a) Analyse the communication challenges that might arise when a CPU interacts with an I/O device like a printer. Propose a solution involving an intermediary system to address these challenges and create a diagram to illustrate your proposed solution.	5	CO3	BL2
	b) Explain how organizing memory into four modules can improve the performance of a memory system with a 16-bit address space. Use sketches to demonstrate the concepts of lower-order and higher-order interleaving. Determine which memory module would store the word at address 0xA2C8 for both schemes and justify your reasoning.	5		