REG.NO

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

SLOT: F1+TF1

Programme Name & Branch	: BTech ECE/CSE
Course Code and Course Name	: BECE102L & Digital System Design
Faculty Name(s)	: PRAYLINE RAJABAI C, ANTONY XAVIER GLITTAS X, SUMIT KUMAR JINDAL, HEMALATHA K, ANAND S, AVINASH CHANDRA, RAGUNATH G, ARUN DEV DHAR DWIVEDI, NAVEEN MISHRA, NIROJ KUMAR SAHU, SHANIDUL HOQUE, MOHIUL ISLAM, LAVANYA N, GEORGE JACOB, HEMANTA KUMAR SAHU, KALYANBRATA GHOSH, VIVEK RAJPOOT, SHILPI RUCHI KERKETTA, SUKANTA KUMAR TULO, ABHISHEK NARAYAN TRIPATHI, RAJESHKUMAR V, SUMATHI G, DILIP KUMAR CHOUDHARY, TANMAYA KUMAR DAS, MANGAIYARKARASI R, ROHIT MATHUR, RAHUL MANOHAR O
Class Number(s)	: VL2025260102573, 2579, 3578, 3580, 3583, 3585, 3587, 3589, 3591, 3593, 3598, 3600, 3603, 3605, 3608, 3610, 3613, 3619,3622,3627,3630,3634,3643,3645,3647,3651,3657
Date of Examination	: 10.10.25
Exam Duration	: 90 minutes (2.00 PM – 03.30 PM) Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes are:

C02: Model the Combinational and Sequential logic circuits using Verilog HDL.
C03: Design the various combinational logic circuits and data path circuits.
C04: Analyze and apply the design aspects of sequential logic circuits.

<table>
<tr><th>S.No.</th><th>Question</th><th>CO</th><th>BL</th><th>Marks</th></tr>
<tr><td>1.</td><td>Write a verilog program in behavioural modelling for the digital circuit which has inputs namely “A” and “B” each of 2-bit wide and generate specific output based on control values i.e., M and N.
<table>
<tr><th>M</th><th>N</th><th>Output</th></tr>
<tr><td>0</td><td>0</td><td>A + B</td></tr>
<tr><td>0</td><td>1</td><td>A + 2B</td></tr>
<tr><td>1</td><td>0</td><td>2A + B</td></tr>
<tr><td>1</td><td>1</td><td>A - B</td></tr>
</table></td><td>2</td><td>BL3</td><td>10</td></tr>
<tr><td>2.</td><td>A combinational circuit has four inputs (A, B, C, and D) and one output Z. The output is ‘1’ if the input has three consecutive 0’s or three consecutive 1’s. Design using 4:1 multiplexer with B & D as the selection lines.</td><td>3</td><td>BL3</td><td>10</td></tr>
</table>

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3.	Construct the logical diagram for a 4 to 2 priority encoder, for which the order of priority as D1>D0>D3>D2 (D1 is the highest priority and D2 is the least priority).	3	BL3	10
4.	Show the steps involved in multiplying −15 with +12 using a 5-bit Booth's multiplier. Determine the final product and the number of addition and subtraction operations performed.	3	BL3	10
5.	The characteristics of G-H flip-flop is given below: If GH = 10, the flip-flop changes state (complement), GH = 11, the flip-flop is set to Q = 1 (set), GH = 00, the flip-flop is set to Q = 0 (reset) and GH = 01 is not allowed (Invalid) (a) Give the characteristic (next-state) equation for the G-H flip-flop. (b) Find the excitation table of G-H flip-flop, using don't-cares where possible. (c) Realize the D flip-flop using the G-H flip-flop.	4	BL3	10

Q_n	Q_{n+1}	G	H
0	0		
0	1		
1	0		
1	1		