VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Engineering
FS_2022-23 (CAT-II)

Course Code : BECE102L **Duration** : 90 Minutes.
Course Name : Digital Systems Design
Faculty Name : SHWETA B THOMAS, ABRAHAM SAMPSON S, ABDUL MAJEED K K, MANIKANDAN SP, ANTONY XAVIER GLITTAS X, JAYANANDAN T, CHITTARANJAN NAYAK, VIKAS VIJAYVARGIYA, NAVEES AHMED S, ANILKUMAR P
Slot : D2+TD2 **Max. Marks** : 50M

Course Outcomes (CO):

CO 1	Optimize the logic functions using and Boolean principles and K-map
CO2	Model the Combinational and Sequential logic circuits using Verilog HDL
CO 3	Design the various combinational logic circuits and data path circuits
CO 4	Analyze and apply the design aspects of sequential logic circuits
CO 5	Analyze and apply the design aspects of Finite state machines
CO 6	Examine the basic architectures of programmable logic devices

S. No	Course Outcomes (CO's) Mapping (CO1-CO6)	CO	Blooms Taxonomy (BL1 –BL6)	Marks Allotted
Q1	(i) Implement the following Boolean function (Y) with an 8 × 1 multiplexer and external NAND gates. **Y (A, B, C, D)** =Π M (0, 1, 2,4,5,6,7,11, 12, 13, 15) (ii) Realize the designed function in part (i) using 4 × 1 multiplexer	CO3	BL3	**10**
Q2	(i) Design a combinational circuit with inputs D0, D1, D2, D3 and outputs X, Y, V. The operation of the combinational circuit must be such that if two or more inputs are equal to 1 at the same time, highest priority input among the inputs is considered. The order of priority is D0>D1>D2>D3. Here V is the valid bit indicator that is set to 1 when one or more inputs are equal to 1. (ii) Write only a test bench in Verilog to verify the design circuit in part (i). Here consider module name is "Priority_Circuit" and inputs D0, D1, D2, D3 and outputs X, Y, V.	CO3 CO2	BL6	**10**

Q3	The outputs of a combinational circuit is defined by the following three Boolean functions: $F1\ (A, B, C) = \sum (1, 4, 6)$ $F2\ (A, B, C) = \sum (3, 5)$ $F3\ (A, B, C) = \sum (2, 4, 6, 7)$ Implement the circuit using 3x8 decoder and NAND gates only.	CO3	BL3	**10**
Q4	A New clocked X-Y flip-flop is defined with two inputs, X and Y is addition to the clocked input. The flip flop functions as follows: If XY=01, the flip flop state (Q) becomes 1 at the next clock pulse If XY=10, the flip flop state (Q) becomes 0 at the next clock pulse. If X=Y, the flip flop toggles its state (Q) at the next clock pulse. i. Provide the truth table for the X-Y flip flop ii. Provide the characteristics table iii. Provide the Excitation table for the X-Y flip flop iv. Implement in X-Y flip flop using a J-K flip flop	CO4	BL5	**10**
Q5	Obtain the Boolean expressions (A>B, A=B and A<B) for 6-bit magnitude comparator and then after model the expression using data flow modelling.	CO3	BL2	**10**

Moderators Remarks:
Q1.
Q2.
Q3.
Q4.
Q5.

Moderator's Signature.

Faculty Response for the Moderators Remarks:
Q1.
Q2.
Q3.
Q4.
Q5.

HOD Signature

Faculty Signature