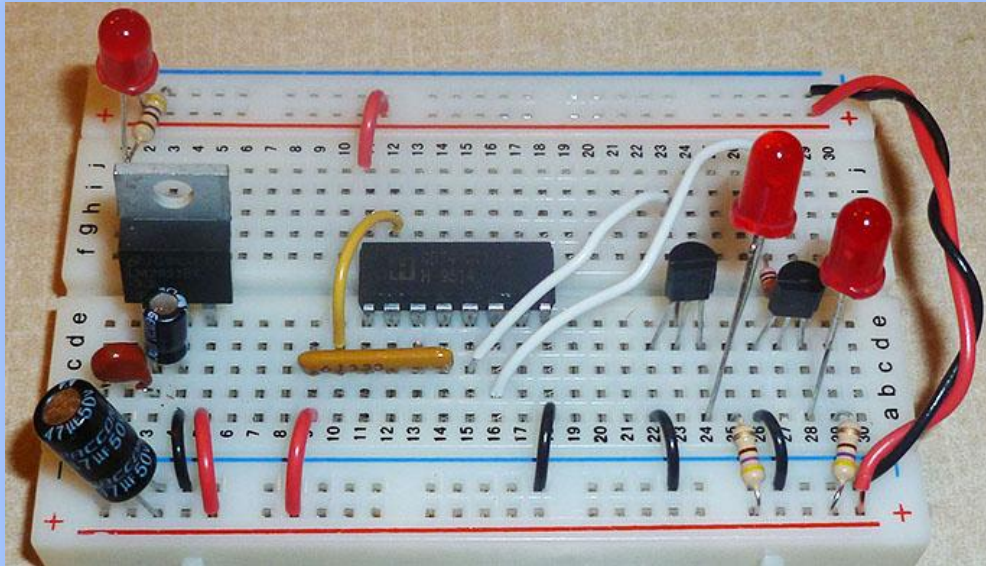




VIT[®]
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING



Laboratory Manual

BEEE102P-Basic Electrical and Electronics Engineering

Name :

Reg. No :

Slot :

Faculty :

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Course Name : Basic Electrical and Electronics Engineering Practical

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Internal Examiner

List of Experiments

Hardware Experiments

Sl.No	Date	Name of the Experiment	Remark
1		Verification of Kirchhoff's voltage law	
2		Staircase wiring circuit layout of multi storage building	
3		Design of half adder circuit using logic gates	
4		Design of regulated power supply using Zener diode	
5		Characteristics of PN Junction diode	

Simulation Experiments

Sl.No	Date	Name of the Experiment	Remark
1		Verification of Kirchhoff's current law	
2		Verification of maximum power transfer theorem using parametric sweep method	
3		Sinusoidal steady state response of RLC series circuit	
4		Design of full adder digital circuit	
5		Design of single-phase half-wave and full wave rectifier	

Hardware Experiments

Ex. No.: 1

Date:

Verification of Kirchhoff's voltage law (KVL)

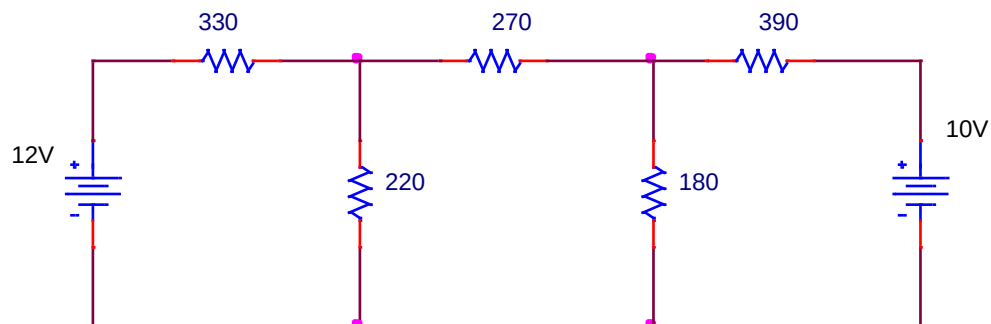
Aim:

To study and verify the Kirchhoff's voltage law for the given network.

Apparatus/Tool required:

Sl. No.	Components Name	Range	Quantity
1	Resister	330 Ω , 270 Ω , 390 Ω , 220 Ω , 180 Ω	Each 1 No.
2	Ammeter	0-50mA (DC)	1 No.
3	Voltmeter	0-30V (DC)	1 No.
4	RPS	0-32 V (DC)	1 No.
5	Connecting Wires	-	Few
6	Bread Board	-	1 No.

Circuit Diagram:



Theory:

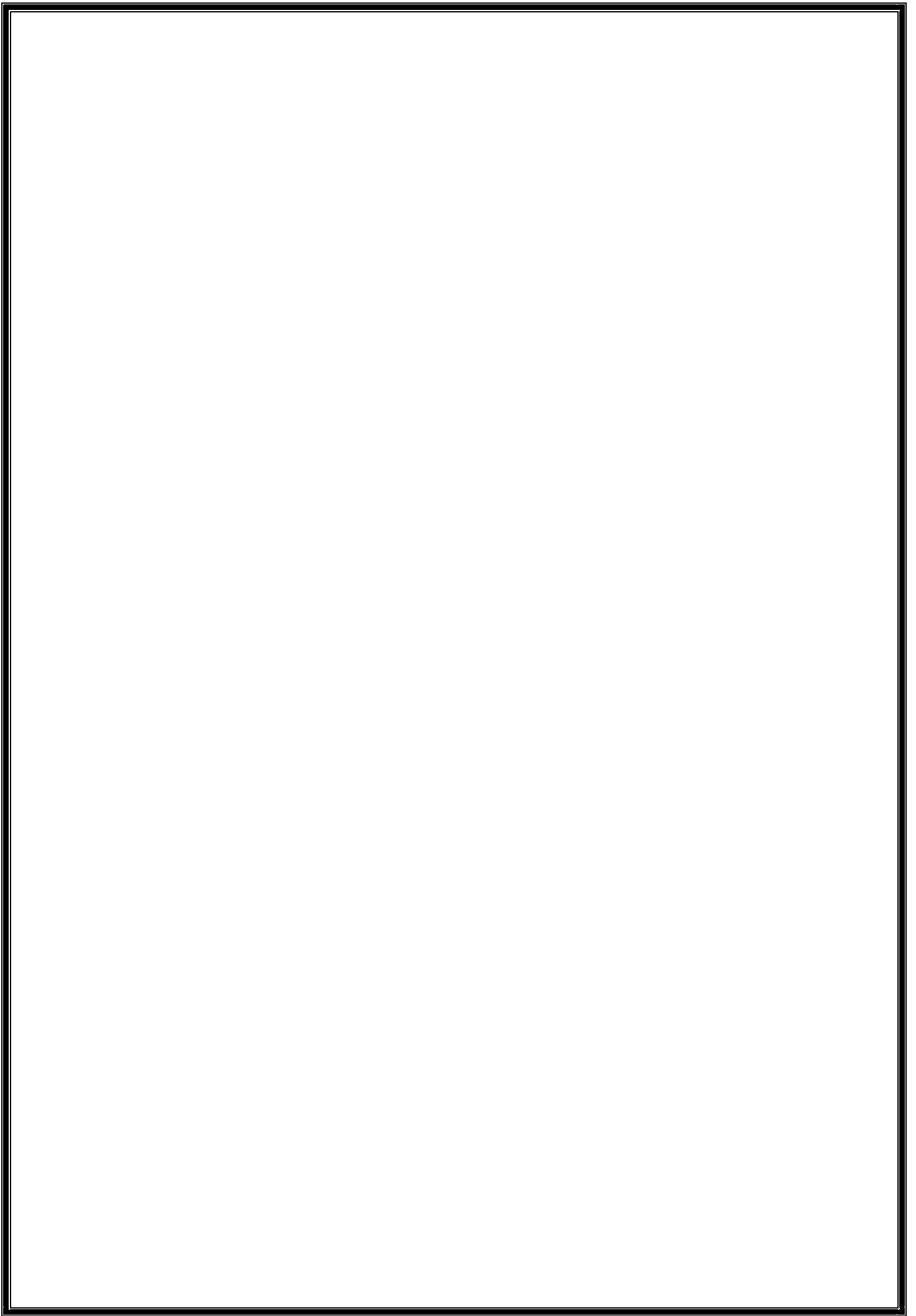
Kirchhoff's Voltage Law (KVL):

It states that in a closed circuit, the algebraic sum of all source voltages must be equal to the algebraic sum of all the voltage drops. Voltage drop is encountered when current flows in an element (resistance or load) from the higher-potential terminal toward the lower potential terminal. Voltage rise is encountered when current flows in an element (voltage source) from lower potential terminal (or negative terminal of voltage source) toward the higher potential terminal (or positive terminal of voltage source).

Manual Calculations:

Practical Circuit

Photograph of practical circuit done in the lab



Procedure:

1. Connect the circuit as shown in the circuit diagram
2. Adjust the voltage sources and set to the required values as shown in the circuit diagram
3. Note down the ammeter and voltmeter reading
4. Find out the branch voltage and currents and compare it with the calculated values

Result:

Manual Calculations

Practical output

Ex. No.: 2

Date:

Staircase wiring circuit layout for multi storage building

Aim:

To control the status of a given lamp from 2 different locations by using two – way switches.

Apparatus/Tool required:

S. No.	Name of the apparatus	Range / Type	Quantity
1	Incandescent Lamp	230 V, 25 W	1 No.
2	Lamp holder	230 V, Level	1 No.
3	Switch Box	4" x 4"	2 Nos.
4	2-way switch	230 V, 5 A	2 Nos.
5	P. V. C. casing capping	1/4"	As required
6	Wooden Board	4' x 3.5'	1 No.
7	Wires	1 sq. mm"	As required

Tools Required

Screw driver, Wire stripper, Hacksaw, combination plier, drilling machine, electrician knife.

Theory

In this wiring, a single lamp is controlled from two places. For this purpose two numbers of two way switches are used. This wiring which makes use of 2 switches to operate bulb at the beginning of the stair lights and the bulb gives off by pushing the button in the end. One of the terminals of the bulb is connected to the main line whose power line is connected to middle slot of two-way switch. Remaining first of these slots is connected in parallel as in crossed node.

Fuse Rating Calculations

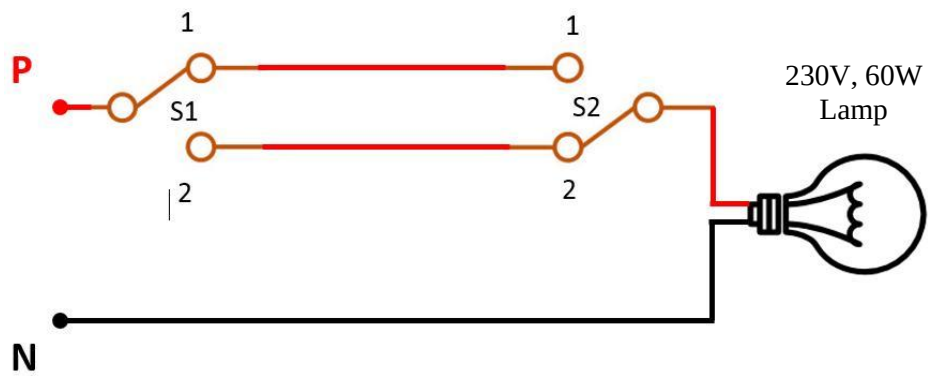
Power drawn by the circuit = 60 watts Voltage of the circuit = 230 volts

$$P = V I \cos \phi$$

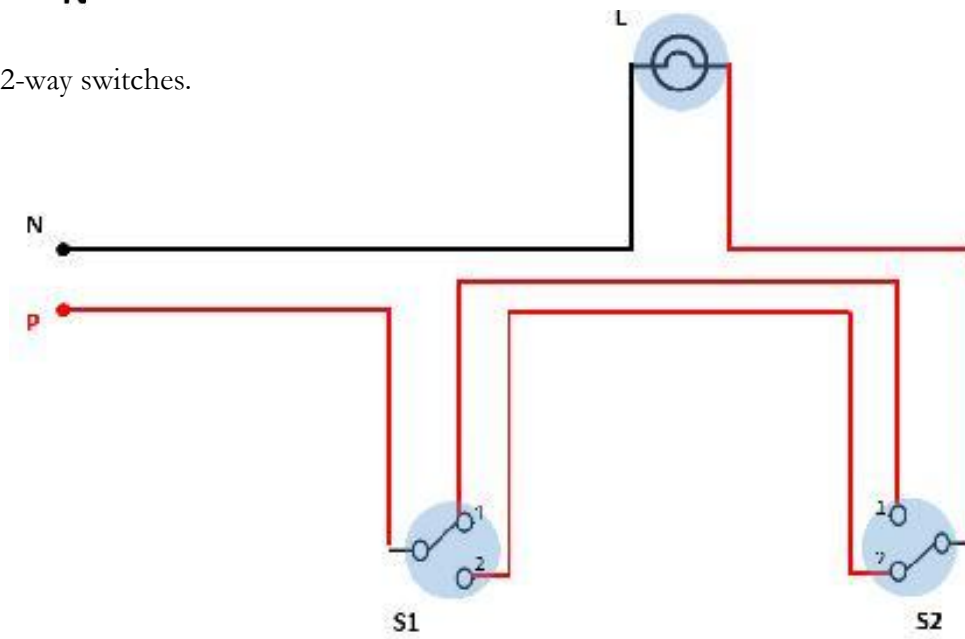
$$P = V \times I \times 1 \text{ (Assuming } \cos \phi = 1 \text{ for resistive load)}$$
$$\text{Current in the circuit (I)} = (\text{power (P)} / \text{Voltage (V)})$$
$$= 60 \text{ W} / 230 \text{ V} = 0.260 \text{ AMP.}$$

Fuse rating of the circuit = rounding off the current to the nearest 5 = 5A (Normally fuses are available in the ratings of 5A, 10A and etc.)

Circuit Diagram



S1, S2 : 2-way switches.



Observation

Condition No	Expected conditions			Observed conditions		
	S1	S2	Lamp	S1	S2	Lamp
1	1	1	ON			
2	1	2	OFF			
3	2	1	OFF			
4	2	2	ON			

Photograph of the practical circuit done in the lab

Procedure

1. Collect the materials required for this experiment.
2. Draw the layout of the given circuit diagram in the circuit board.
3. Fix the necessary materials, by using drilling machine in the layout board.
4. One end of the lamp holder is connected to neutral point and another point is connected at the center of the two-way switch (S2)
5. The center of the switch (S1) is connected to the phase line.
6. The connection of the other two ends of two-way switch is connected as follows. The point 1 of switch S1 is connected to point 1 of switch S2 and point 2 of S1 is connected to point 2 of S2.
7. The given lamp is fixed on the lamp holders.
8. Test the Circuit for all possible combination of switch positions.

Precautions

1. Energize the circuit with the presence of Lab instructor / Faculty.
2. No part of a live circuit should be touched by the bare hand.
3. Keep the body, or any part of it, out of the circuit.
4. Keep the work area and workbench clear of items not used in the experiment.
5. When disassembling a circuit, first remove the source of power.

Result

Ex. No.: 3

Date:

Design of half adder circuit using logic gates

Aim:

To design and verify a half adder using logic gates

Apparatus/Tool required

S. No.	Name of the apparatus	Range / Type	Quantity
1	IC 7486	-	1 No.
2	IC 7408	-	1 No.
3	LED	-	2 Nos.
4	RPS	0 – 15 V	1 No.
5	Resistor	330 Ω	2 Nos.
6	Breadboard	-	1 No.
7	Wires	-	Few

Theory

Half adder circuit is two-bit adder. It is also known as modulo – 2 adder. The expression for logic sum S of half adder is

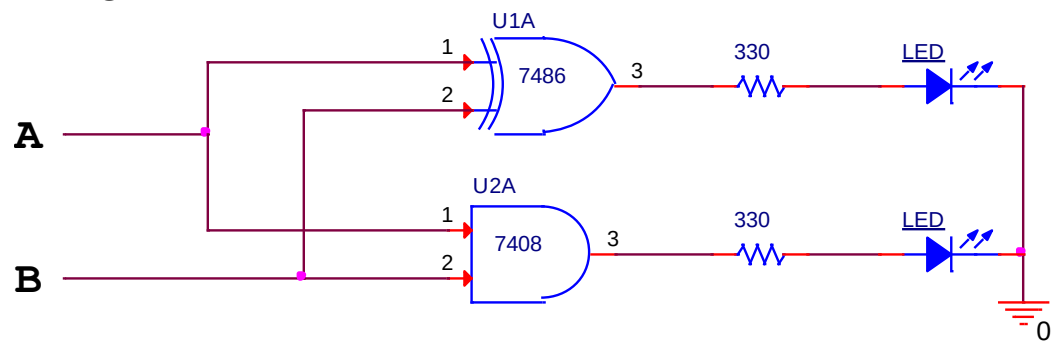
$$S = A\bar{B} + \bar{A}B = A \oplus B$$

The logic expression for carry C is

$$C = A \cdot B$$

Inputs		Outputs	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Circuit Diagram:



Photograph of the practical circuit done in the lab

Truth Table

A	B	$S=A\oplus B$	$C=A.B$
0	0		
0	1		
1	0		
1	1		

Procedure:

1. Connect the circuit as shown in figure
2. Apply voltages to inputs A and B as represented in the truth table and verify the truth table

Result:

Ex. No.: 4

Date:

Design of regulated power supply using Zener diode

Aim:

To verify the performance of Zener diode

Apparatus/Tool required

S. No.	Name of the apparatus	Range / Type	Quantity
1	Zener diode	-	1 No.
2	RPS	0 – 30 V	1 No.
3	Voltmeter	0 – 30 V	2 No.
4	Resistor	330 Ω	1 No.
5	Resistor	1 k Ω	1 No.
6	Breadboard	-	1 No.
7	Wires	-	Few

Theory

Zener diodes are generally used in the reverse bias mode. This voltage across the diode (Zener Voltage, V_z) remains nearly constant even with large changes in current through the diode caused by variations in the supply voltage or load. This ability to control itself can be used to great effect to regulate or stabilize a voltage source against supply or load variations. The Zener diode maintains a constant output voltage until the diode current falls below the minimum I_z value in the reverse breakdown region, which means the supply voltage, V_s , must be much greater than V_z for a successful breakdown operation. When no load resistance, R_L , is connected to the circuit, no load current ($I_L = 0$), is drawn and all the circuit current passes through the Zener diode which dissipates its maximum power. So, a suitable current limiting resistor, (R_s) is always used in series to limit the Zener current to less than its maximum rating under this "no-load" condition.

As shown in the circuit diagram, a more stable reference voltage can be produced by connecting a simple Zener regulator circuit across the output of the rectifier. The breakdown condition of the Zener can be confirmed by calculating the Thevenin voltage, V_{TH} , facing the diode is given as:

$$V_{TH} = \frac{R_L}{R_s + R_L} V_s$$

This is the voltage that exists when the Zener is disconnected from the circuit. Thus, V_{TH} has to be greater than the Zener voltage to facilitate breakdown. Now, under this breakdown condition, irrespective of the load resistance value, the current through the current limiting resistor, I_S , is given by

$$I_S = \frac{V_S - V_Z}{R_S}$$

The output voltage across the load resistor, V_L , is ideally equal to the Zener voltage and the load current, I_L , can be calculated using Ohm's law:

$$V_L = V_Z \text{ and } I_L = \frac{V_L}{R_L}$$

Thus the Zener current, I_Z , is

$$I_Z = I_S - I_L.$$

Now that you have constructed a basic power supply, its quality depends on its load and line regulation characteristics as defined below.

Load Regulation: It indicates how much the load voltage varies when the load current changes. Quantitatively, it is defined as:

$$\text{Load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

where V_{NL} = load voltage with no load current ($I_L = 0$) and V_{FL} = load voltage with full load current. The smaller the regulation, the better is the power supply.

Line Regulation: It indicates how much the load voltage varies when the input line voltage changes. Quantitatively, it is defined as:

$$\text{Line regulation} = \frac{V_{HL} - V_{LL}}{V_{LL}} \times 100\%$$

where V_{HL} = load voltage with high input line voltage, and V_{LL} = load voltage with low input line voltage. As with load regulation, the smaller the regulation, the better is the power supply.

Circuit Diagram

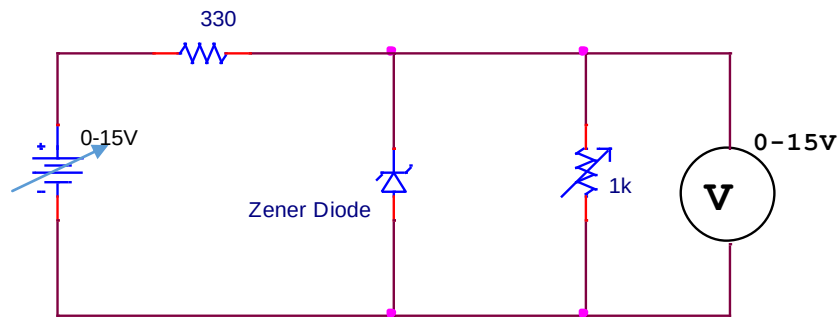


Table (i) Line Regulation: Load Resistor = _____ Ω

Sl.No	Input DC Voltage (V_i) in Volts	Output DC Voltage (V_L) in Volts
1		
2		
3		
4		
5		
6		

Table (ii) Load Regulation: Input d.c. voltage = _____ V

Sl.No	Load Resistance in ohms	Output DC Voltage (V_L) in Volts
1		
2		
3		
4		
5		
6		

Photograph of the practical circuit done in the lab

Procedure:**Line Regulation:**

1. Connect the circuit as shown in the diagram
2. Keep the load resistance constant at a particular value
3. Vary the input voltage and note down the variation in the output voltage

Load Regulation:

1. Connect the circuit as shown in the diagram
2. Keep the input voltage constant at a particular value
3. Vary the load resistance and note down the variation in the output voltage

Result:

Ex. No.: 5

Date:

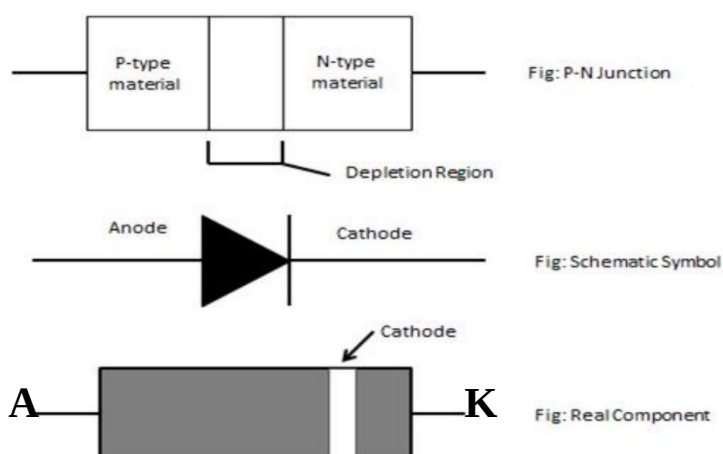
Characteristics of PN Junction Diode

Aim:

Apparatus/Tool required:

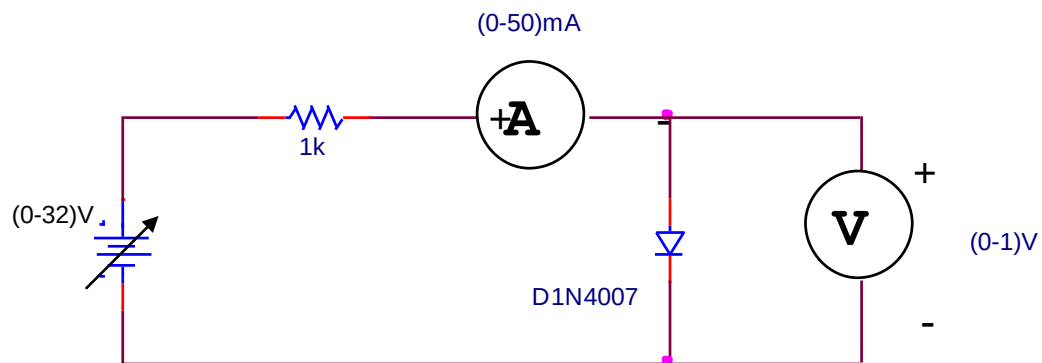
Sl. No.	Components Name	Range	Quantity
1	Resister	1k Ω , 470 Ω	1 No.
2	PN Junction Diode	D1N4007	1 No.
3	RPS	0-32 V (DC)	1 No.
4	Ammeter	(0-50)mA, (0-500) μ A	Each 1 No.
	Voltmeter	(0-1)V, (0-10)V	Each 1 No.
5	Connecting Wires	-	Few
6	Bread Board	-	1 No.

Identification of Terminals:

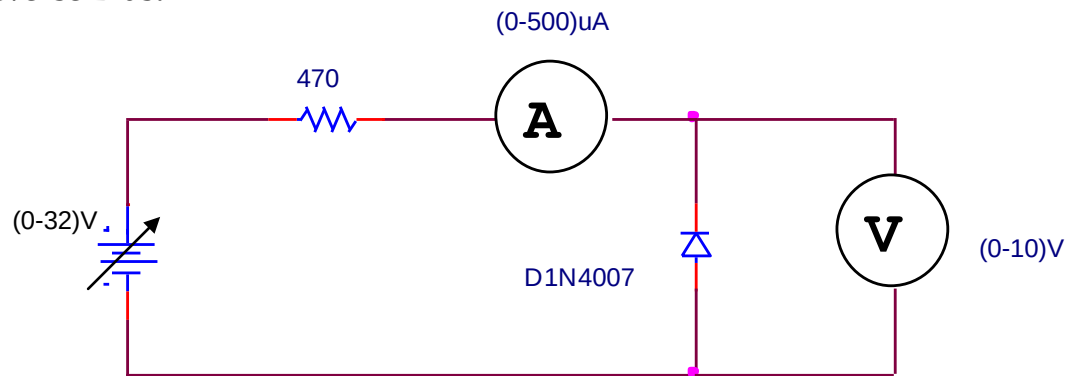


Hardware Circuit Diagram:

Forward Bias:

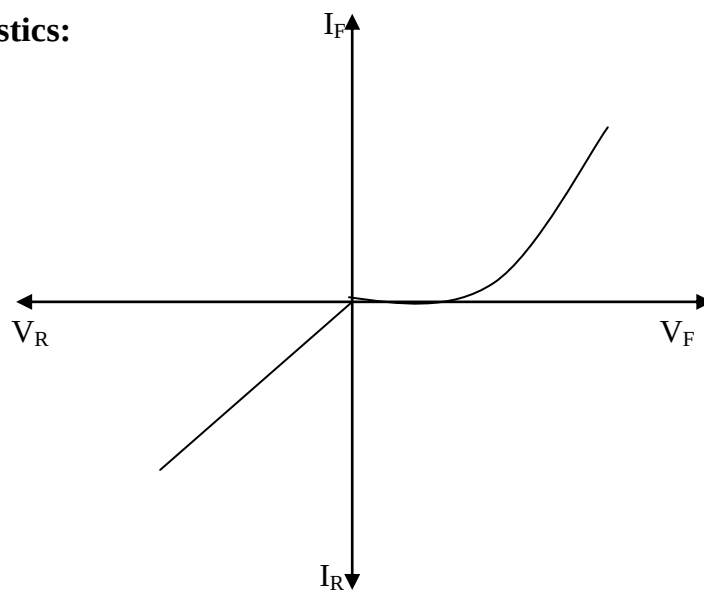


Reverse Bias:



Model Graph:

V-I Characteristics:



Theoretical Circuit Diagram:

Forward Bias:

Reverse Bias:

Virtual Lab Tabulations:

Forward Bias:

[illegible]

Reverse Bias:

[illegible]

VI Characteristics

Forward Bias:

Reverse Bias:

Result:

Software Experiments

Ex. No.: 1

Date:

Verification of Kirchhoff's current law (KCL)

Aim:

To study and verify the Kirchhoff's laws for the given Network.

Software /Tool required:

ORCAD / Capture CIS --> **Analog Library – R**
 Source Library – Vdc
 Ground (GND) – 0 (zero)

Simulation Settings: **Analysis Type – Bias point**

Circuit Diagram:

Theory:

Kirchhoff's Current Law (KCL)

KCL states that at any node (junction) in a circuit the algebraic sum of currents entering and leaving a node at any instant of time must be equal to zero. Here currents entering (+ve sign) and currents leaving (-ve sign) the node must be assigned opposite algebraic signs.

Photograph of practical circuit done in the lab

Manual Calculations:

Procedure:

- 1) Open orCAD Tool and create new project.
- 2) Draw the circuits (mesh and nodal) using the tools: R analog, VDC source, IDC source, connecting wire and a ground potential.
- 3) Enter the values in R, V and I.
- 4) Go to PSpice and create a new simulation profile.
- 5) In the simulation settings dialogue box, chose analysis type as Bias Point, enter APPLY and OK.
- 6) Now click Run PSpice.
- 7) Enable bias voltage display and Enable bias current display.
- 8) Compare the values to the manually calculated values and write the result.

Result:

	Manual Calculations	Practical output
V_A		
I_1		
I_2		
I_3		

Ex. No.: 2

Date:

Verification of maximum power transfer theorem

Aim:

To study and verify Maximum Power Transfer Theorem.

Software /Tool required:

ORCAD / Capture CIS --> **Analog Library – R**
 Source Library – Vdc , Idc etc.
 Ground (GND) – 0 (zero)

Simulation Settings: **Analysis Type – Bias point , DC Sweep**

Circuit Diagram:

Theory

Maximum power is developed in a load when the load resistance equals the Thevenin resistance of the source to which it is connected

All linearly constructed sources can be reduced to their Thevenin equivalent. In DC circuits, the load can be represented by a resistance R_L . The source develops a voltage V_L across the load and enables current I_L to flow into it. The power delivered to the load resistance (R_L) depends on the value of R_L . Maximum current I_L occurs when $R_L = 0$ (shorted terminals). The maximum voltage V_L occurs when $R_L = \infty$ (open circuited terminals). Yet load power $P_L = 0$ for both cases.

P_L is maximum when R_L equals the Thevenin equivalent resistance of the source, i.e. when $R_L = R_{TH}$

Manual Calculation

To find V_{TH}

To find R_{TH}

To find Power across R_L

Photograph of practical circuit done in the lab

To find V_{TH}

To find R_{TH}

To find Power across R_L

Procedure:

- 1) Open OrCAD Tool and create new project.
- 2) Draw the circuits (V_{th} and R_{th}) using the tools: R analog, V_{DC} source, I_{DC} source, connecting wire and a ground potential.
- 3) Enter the values in R and V.
- 4) Go to PSpice and create a new simulation profile.
- 5) In the simulation settings dialogue box, chose analysis type as Bias Point, enter APPLY and OK.
- 6) Now click Run PSpice.
- 7) Enable bias voltage display and Enable bias current display.
- 8) Now draw the Thevenin's equivalent circuit using the tools: R analog, VDC source, ground potential and connecting wire.
- 9) After drawing the circuit, go to Part and chose PARAM/SPECIAL.
- 10) Place it beside the circuit and double click on PARAMETER.
- 11) In the schematic tab, click on pivot and then click on new property.
- 12) Now enter name as Rvar and value as 1. Enter APPLY and OK.
- 13) Go to PSpice and create a new simulation profile.
- 14) In the simulation settings dialogue box, chose analysis type as DC Sweep, chose sweep variable as global parameter, enter parameter name as Rvar. Under sweep type, enter start value =1, end value = 20 and increment = 0.2. Enter APPLY and OK.
- 15) Chose power dissipation marker and put it on Rvar.
- 16) Now click Run PSpice.
- 17) A different window will open up with a graph containing peak value, R_{th} (x coordinate) and P_{max} (y coordinate).
- 18) Compare the values to the manually calculated values and write the result.

Graph obtained using PSPICE

Result:

Calculated Value

Simulated Value

Ex. No.: 3

Date:

Sinusoidal steady state response of RLC circuit

Aim:

To find the resonance frequency of a RLC circuit using OrCAD tool

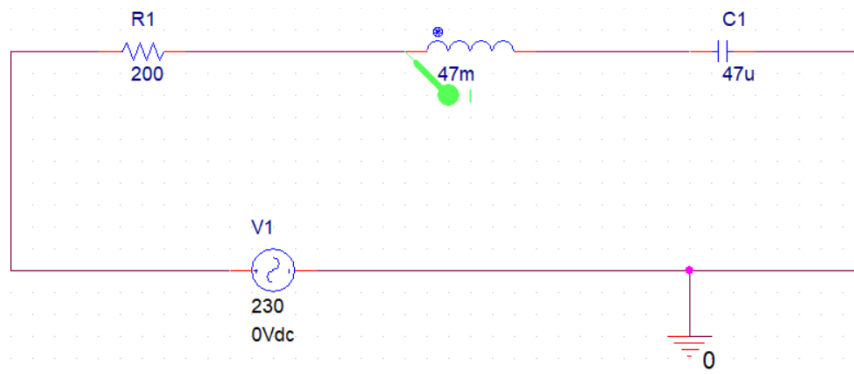
Software /Tool required:

ORCAD / Capture CIS --> Analog Library – R, L & C

Source Library – Vac , Ground (GND) – 0 (zero)

Simulation Settings : Analysis Type – AC Sweep

Circuit Diagram:



Theory:

For an RLC circuit, $Z = \sqrt{R^2 + (X_L - X_C)^2}$

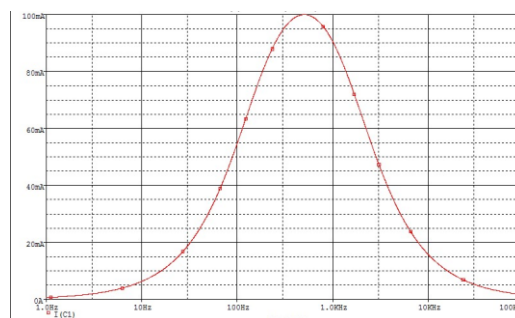
When $X_L = X_C$; Z is minimum.

$I = \frac{V}{Z}$ is maximum

The frequency found when $X_L = X_C$ is called resonance frequency.

Formulae:
$$f = \frac{1}{2\pi\sqrt{LC}}$$

Model Graph



Photograph of practical circuit and Graph obtained in Lab

Procedure:-

- 1) Open OrCAD Tool and create new project.
- 2) Draw the circuits using the tools: R analog, L analog, C analog, VAC/source, connecting wire and a ground potential.
- 3) Enter the values in R, L, V and C.
- 4) Go to PSpice and create a new simulation profile.
- 5) In the simulation settings dialogue box, chose analysis type as AC Sweep. Under AC sweep type, enter start frequency=0.1, end frequency=100000 and points/decade=100. Now enter APPLY and OK.
- 6) Take the current marker and place at the point between wire and the inductor.
- 7) Now click Run PSpice
- 8) A different window with a bell-shaped curve opens up with its peak giving us the resonance frequency (x coordinate) and resonance current (y coordinate).
- 9) Compare the values to the manually calculated values and write the result.

Result:-

Ex. No.: 4

Date:

Design of full adder digital circuit

Aim:

To design and verify FULL ADDER digital circuit truth table

Software / Tools Required:

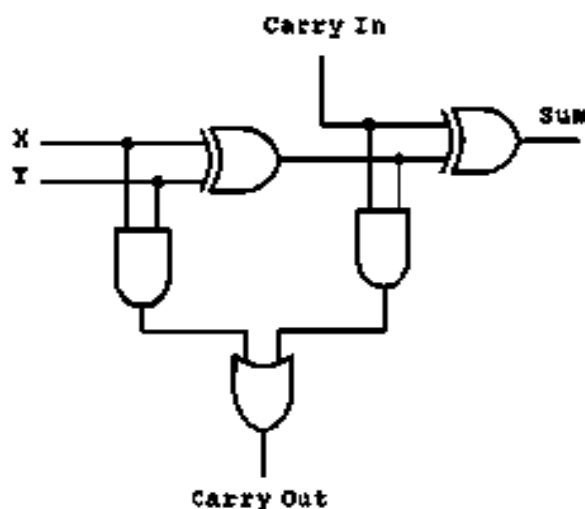
ORCAD / PSpice simulator – AND GATE: 7408

OR GATE: 7432

XOR GATE: 7486

Simulation Settings: Time domain (Transient)

Circuit diagram



Theory:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs (X,Y and Carry In) and two outputs(Sum and Carry Out). A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

$$\text{SUM} = \bar{x}\bar{y}C_{in} + \bar{x}y\bar{C}_{in} + x\bar{y}\bar{C}_{in} + xyC_{in}$$

$$\bar{C}_{in}(\bar{x}y + x\bar{y}) + C_{in}(\bar{x}\bar{y} + xy)$$

$$\begin{aligned} & \overline{Cin}(x \oplus y) + Cin(\overline{x \oplus y}) \\ = & (x \oplus y) \oplus Cin \end{aligned}$$

$$\begin{aligned} \text{Carry Out} = & x\overline{y}Cin + x\overline{y}Cin + \overline{x}yCin + \overline{x}y\overline{Cin} \\ = & Cin(x\overline{y} + \overline{x}y) + xy(Cin + \overline{Cin}) \\ & Cin(x \oplus y) + xy \end{aligned}$$

Inputs			Outputs	
X	Y	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

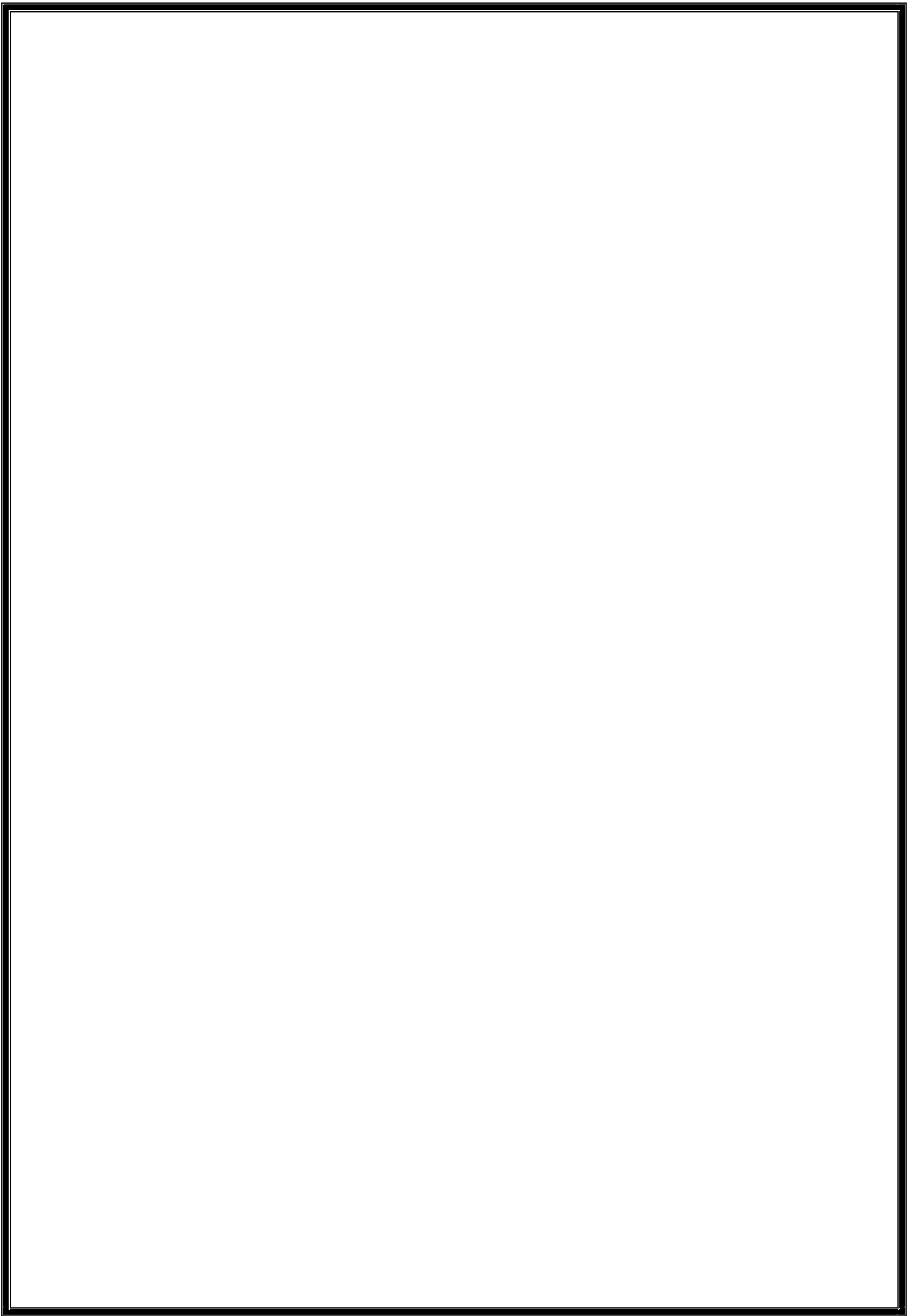
Photograph of practical circuit done in Lab

Timing Diagram obtained in Lab

Procedure:

1. Open OrCAD and create a new project.
2. Draw the circuits using the parts given in apparatus required, digclock/source and the connecting wires.
3. In digclock, Enter 1: offtime = ontime = 1ms ; 2: offtime = ontime = 2ms ; 3: offtime = ontime = 4ms
4. Create a new simulation profile in pspice. In simulation settings: chose analysis type as time domain(transient) and set run to time = 8ms.
5. Click apply and ok.
6. Now take the voltage probe and put it at the input and output end of the circuit.
7. Click run. Note down the graph and the circuit in the manual.

Result:



Ex. No.: 5

Date:

Realization of single-phase rectifier circuit

Aim:

To Design Half wave and Full wave Rectifier Circuit in Pspice simulation.

Software /Tool required:

ORCAD / PSpice simulator -> Diode Library - D1N4002/4007,

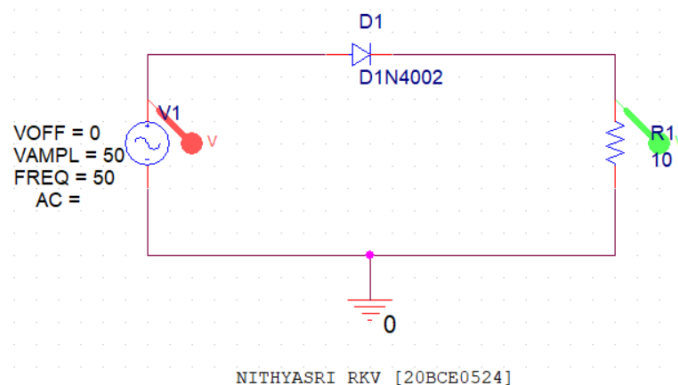
Source Library – Vsin & Ground (GND) – 0(zero) Analog Library – R

Simulation Settings: Analysis Type - Time Domain

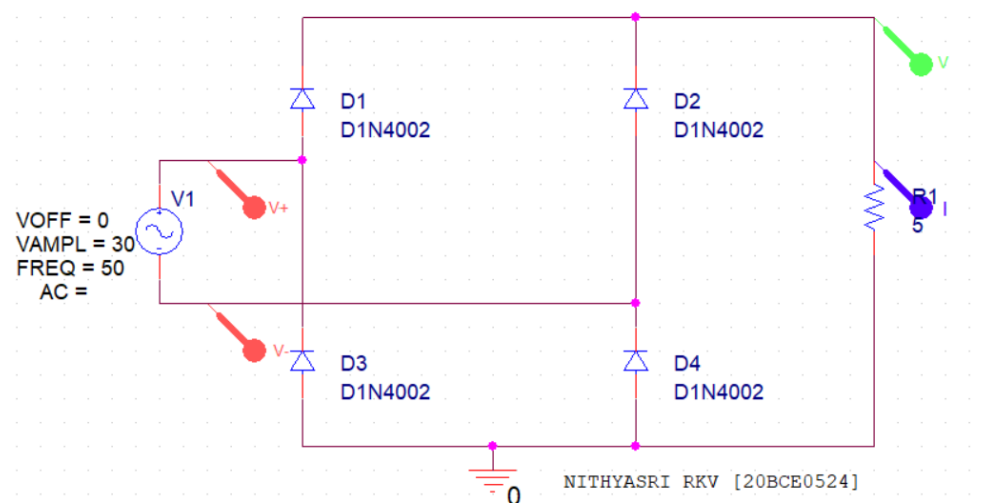
Run to time: 40ms (for 2 cycles)

Circuit Diagram:

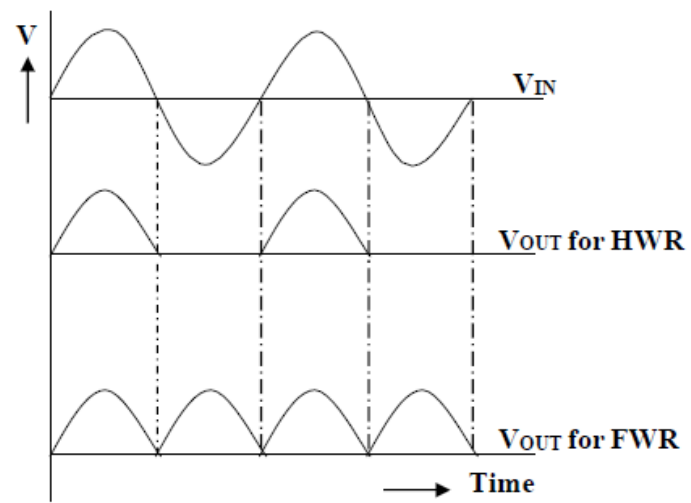
Single phase Half – wave Rectifier



Single phase Full – wave Rectifier



Model Graph:



Photograph of practical circuit and Graph obtained in Lab

Single phase half wave rectifier

Single phase full wave rectifier

Procedure

1. Create the given circuit diagram in new project file using the general procedure.
2. Create New Simulation Profile and select Time Domain (Transient).
3. Give the run time for two cycles, (i.e. 0.04 seconds for 50Hz frequency for two cycles) and press OK.
4. Select the voltage differential marker and connect across the input voltage source and load resistor.
5. Run the simulation and observe the input and output signal variation.

Result: