VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Winter Semester 2022-2023 Continuous Assessment Test – II

Programme Name &Branch: BCB, BCE, BCI, BCT, BDS, BKT **SLOT:** A2+TA2

Course Name & code: Computer Architecture and Organization- BCSE205L

Class Number (s): VL2022230502972, VL2022230504131

Faculty Name (s): Prof. AJITHA D, Prof. VENKATA PHANIKRISHNA B

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s): Answer all five questions

Q. No	Question	Max Marks	CO	BL
1.	A) In One Address Instruction Format, how one operand is sufficient. Is it better than the 0-address instruction format? Explain with proper justification. **[4 Marks]** B) If the CPU employs the One Address Instruction Format to carry out the **X = (M + N × O) / (P × Q)** operation and the variables X, M, N, O, P, and Q are present in memory, then specify all required instructions to evaluate it. (Note: Use only One Address Instruction Format.) **[6 Marks]**	10 [4 + 6]	CO1	BL5
2.	A) How control unit is different from ALU in the CPU? **[4 Marks]** B) Specify different types of control units and compare them in following perceptive **[6 Marks]** i) Cost point of view ii) Instruction counts point view iii) Speed point of view	10 [4 + 6]	CO1	BL3
3.	A) Explain the limitations of MIPS and MFLOPS **[4 Marks]** B) Calculate the CPU execution time if the processor's clock rate is 500 MHz, there are 50000 instructions to execute, and each instruction requires 2.5 CPU cycles to complete. **[6 Marks]**	10 [4 + 6]	CO1	BL4
4.	Design 256 × 16 – bit RAM using 256 × 8 – bit RAM chips and 256 × 8 – bit ROM using 128 × 8 – bit ROM chips A. How many RAM and ROM chips are required? **[2 Marks]** B. Give the address range in hexadecimal for RAM, ROM **[3 Marks]** C. Draw a memory-address map for the system **[5 Marks]**	10	CO3	BL5
5.	A) What is the problem in cache memory direct mapping, Explain with example? **[4Marks]** B) What is the RAM capacity if the number of address lines is five? Using "Consecutive words in a module" and "Consecutive words in a Consecutive module" divide this memory into 4 equal memory blocks. After that, describe how the CPU will locate memory blocks and specific words (or locations in memory) within those memory blocks? **[6Marks]**	10 [4 + 6]	CO3	BL5