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VIT

Vellore Institute of Technology

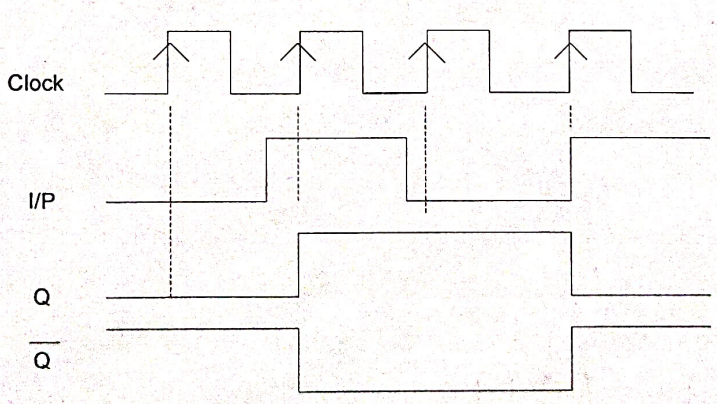
(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering

WEI_2022-23 (CAT-II)

Course Code	: **BECE102L**	**Duration : 90 Minutes.**
Course Name	: **Digital Systems Design**	
Class Numbers	: **VL2022230506857**	
Faculty Name	: **Dr. Abhishek N. Tripathi**	
Slot	: **X11+X12+X21**	**Max. Marks : 50M**

Answer all the questions

S. No.	Questions	Mark
1	Implement the following Boolean function with 4 x1 multiplier and external gates. $F = \Sigma m(0,2,4,5,7,9,11,13,15)$ Connect inputs A and B to the selection lines and the remaining input connections of C and D to the data inputs.	10
2	A digital circuit has three inputs a, b, and c, where a is the MSB and c is the LSB bit, and one output f. When MSB bit is zero it performs the addition of two other input bits and when MSB bit is one it performs the subtraction of two other input bits. Write the Verilog code using behavioural model along with the test bench to implement this logic.	10
3	Design a combinational circuit with four inputs a, b, c and d, and four outputs O1, O2, O3, and O4 using a decoder and gates. When the binary input is less than 10, the binary output is five greater than the input. When the binary input is greater than the 10, the binary output is five less than the input.	10
4	Implement the binary equivalent multiplication of two signed number (7 x -4) with the necessary steps. Explain the step by step procedure to implement it.	10
5	Identify the type of flip flop characterised by the timing diagrams shown in the following Figure. Convert it into D flip flop. Explain the procedure in detail.  	10