VIT
Vellore Institute of Technology

SLOT -E2

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST – II - FALL SEMESTER 2021-2022

Programme Name & Branch: B.Tech & ECE **Class Number(s):** 5844, 5984, 5973

Course Code: BEEE102L **Course Name:** Basic Electrical and Electronics Engineering

Faculty Name(s): Dr Arunachalam V, Dr Govardhan K & Dr Shanidul Hoque

Exam Duration: 90 minutes **Maximum Marks: 50**

Answer all the questions, Open Book Type
Course Outcome (CO), Blooms Taxonomy Level (BL)

S.No.	Question	Marks	CO	BL
1.	Figure 1 shows an iron core whose relative permeability is 2, 000. The dimensions of the core are shown in the figure. The width of the core is 7 cm. The lengths of the air gaps are 0.05 cm and 0.07 cm, respectively. The cross-section in the air gaps is 5% bigger than the iron core. The coil has 300 turns, and its current is 1.0 A. Determine the magnetic flux in each column of the iron core and the magnetic induction in the air gaps.	10	2	5

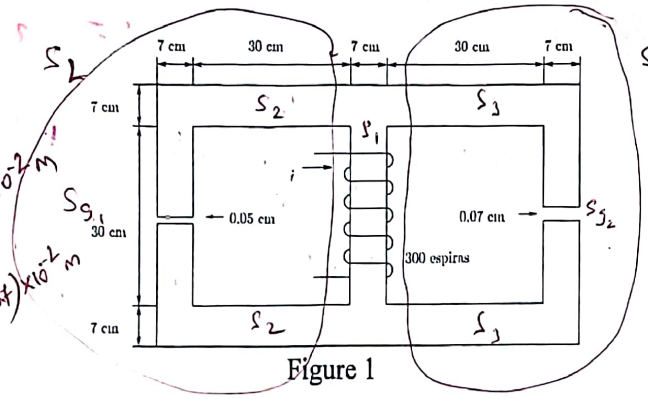


Figure 1

2 (a)	A horizontal straight wire 10 m long extending from east to west is falling with a speed of $5ms^{-1}$, at right angles to the horizontal component of the earth's magnetic field, $0.30 \times 10^{-4}\ Wb/m^2$ i. What is the instantaneous value of the emf induced in the wire? ii. What is the direction of the emf? iii. Which end of the wire is at the higher electrical potential?	05	2	5
2 (b)	A pair of adjacent coils has a mutual inductance of 1.5 H. If the current in one coil changes from 0 to 20 A in 0.5 s, what is the change of flux linkage with the other coil?	05	2	5
3 (a)	Convert the following (i) $(3102.123)_4 \approx (?)_{10}$ (ii) $(AF0C9)_{16} \approx (?)_8$ (iii) $(1110101000111011.001101010010)_2 \approx (?)_8$ (iv) $(1110101000111011.001101010010)_2 \approx (?)_{16}$ (v) $(1562.932)_{10} \approx (?)_4$	05	4	3

3 (b) Perform the following arithmetic using signed-magnitude representation, biased representation and 2's complement: 4 3

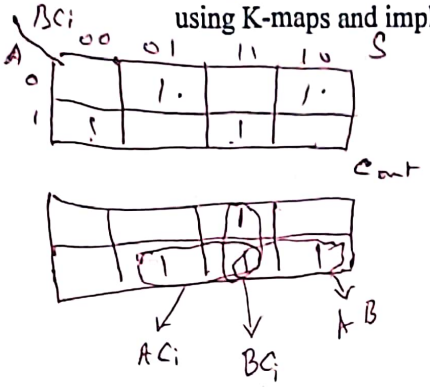
(i) $(+01101.1011)_2 + (-11001.0101)_2 = (?)_2$

(ii) $(-1101.10101)_2 + (+1001.01101)_2 = (?)_2$

-1011.1010

-1000.1000

4 Design a Full adder circuit (functions as per the following truth table) using K-maps and implement using 2-input NOR gates. 10 4 5

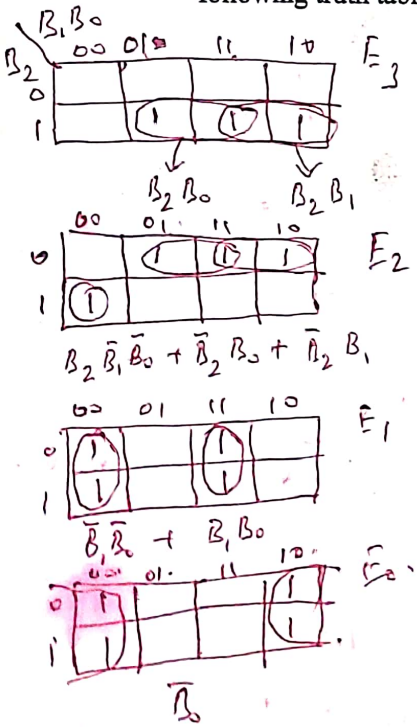


A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = A \oplus B \oplus C$

$C_0 = AB + B C_{in} + A C_{in}$

5 Design a 3-bit binary to 4-bit Excess-3 code (functions as per the following truth table) converter circuit using AND, OR and NOT gates. 10 4 5



Binary			Excess-3			
B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

$E_3 = B_1 B_2 + \overline{B_0} \cdot B_2$

$E_2 = \overline{B_1} \overline{B_2} + B_0 \overline{B_2} + \overline{B_0} \overline{B_1} \overline{B_2}$

$E_1 = B_0 B_1 + \overline{B_0} \overline{B_1}$

$E_0 = \overline{B_0}$