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Vellore Institute of Technology

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SCHOOL OF ELECTRONICS ENGINEERING

CONTINUOUS ASSESSMENT TEST I, WINTER 2022-23

BECE102L- Digital Systems Design

Time: 1.30 Hrs. Slot: C2+TC2 Max. Marks: 50

Faculty(s): Anand S, Swati G, George Jacob

Answer All Questions

1.	a.	Prove the following Boolean Expression $$[A\bar{B}(C+BD)+\bar{A}\bar{B}]=\bar{B}C$$ In this question, there is a literal C missing to prove this expression. $$[A\bar{B}(C+BD)+\bar{A}\bar{B}]C=\bar{B}C$$ So steps to simplify the expression using Boolean algebra are considered for correction. $A\bar{B}C+A\bar{B}BD+\bar{A}\bar{B}$ $A\bar{B}C+\bar{A}\bar{B}$ $\bar{B}(AC+\bar{A})$ $\bar{B}(\bar{A}+C)$ $\bar{A}\bar{B}+\bar{B}C$	[5]
	b.	Simplify the expression $Y=(A+B)\left(\overline{\bar{A}(\bar{B}+\bar{C})}\right)+\bar{A}(B+C)$ as much as possible using Boolean Algebra. Simplify, $Y=(A+B)(A'(B'+C'))'+A'(B+C)$ *Solution* $Y=(A+B)((A+(B'+C')')+A'(B+C)$: De Morgan's theorem $=(A+B)(A+BC)+A'(B+C)$: De Morgan's theorem $=(AA+ABC+AB+BBC)+A'(B+C)$ Distributive law $=(A+AB+ABC+BC)+A'(B+C)$ A.A = A, and B.B = B $=A(1+B+BC)+BC+A'(B+C)$ B + BC = B and 1 + B = 1 $=A+BC+A'(B+C)$ $=(A+A'(B+C))+BC$ A + A'(B + C) = A + (B + C) bec. A + A'B = A +B $=A+B+C+BC$ $=A+B+C(1+B)$ $=A+B+C$	[5]
2.		Reduce the following expression and implement the circuit using AOI, only NAND, and only NOR gates.	[10]

$$F(x, y, z) = \Sigma m(0,4,6,7)$$

Mark distribution [2 + 2 + 3 + 3]

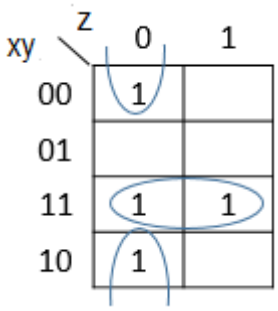
a)

$$\bar{x}\bar{y}\bar{z} + x\bar{y}\bar{z} + xy\bar{z} + xyz$$

$$(\bar{x} + x)\bar{y}\bar{z} + xy(z + \bar{z})$$

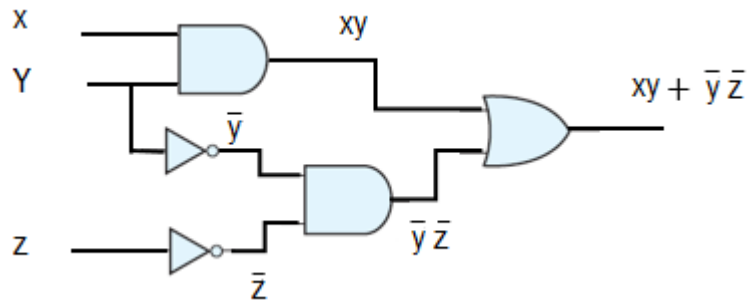
$$\bar{y}\bar{z} + xy$$

OR

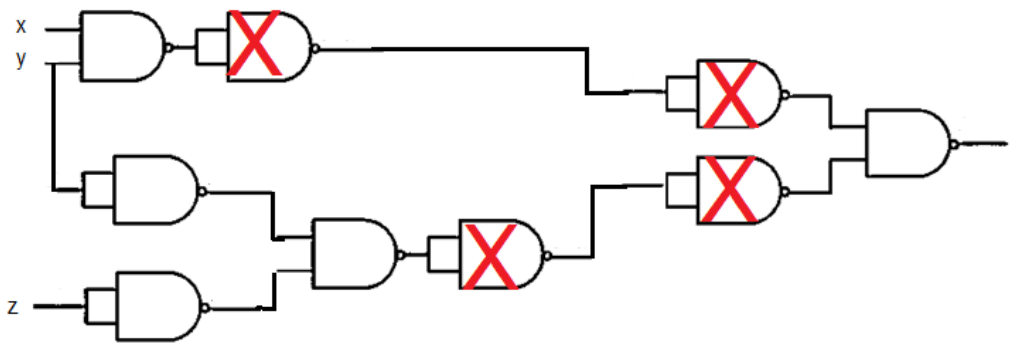


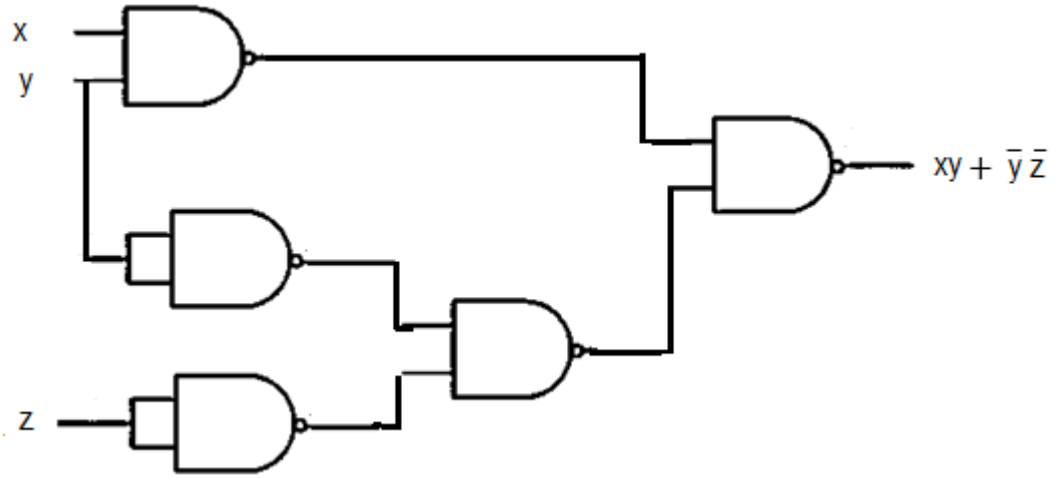
$$\bar{y}\bar{z} + xy$$

b)



c)





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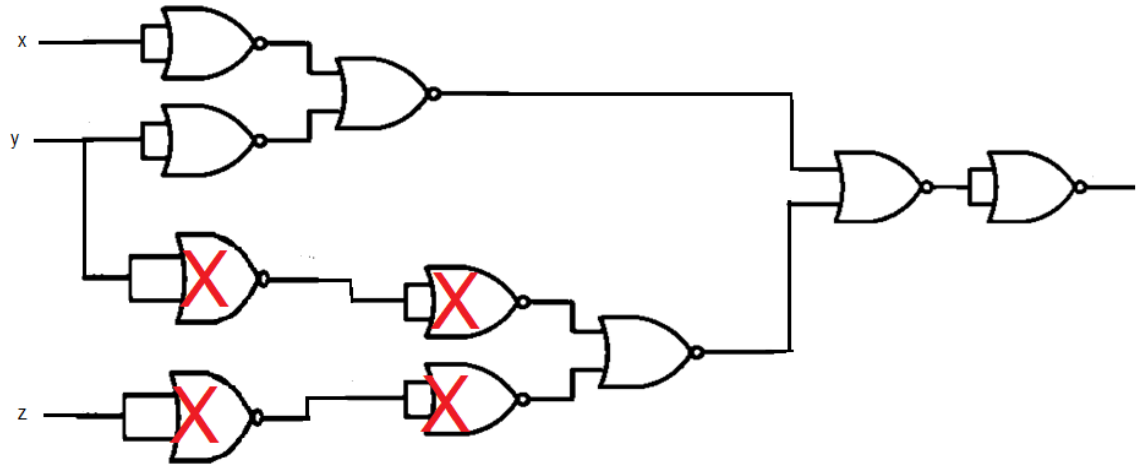
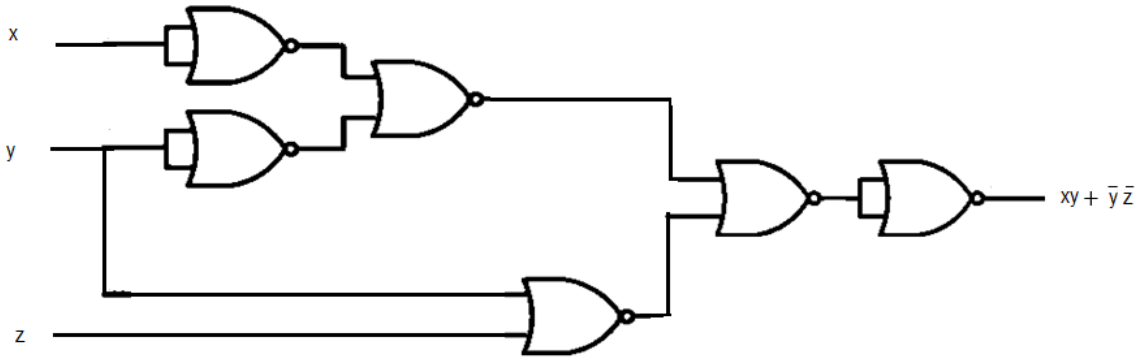




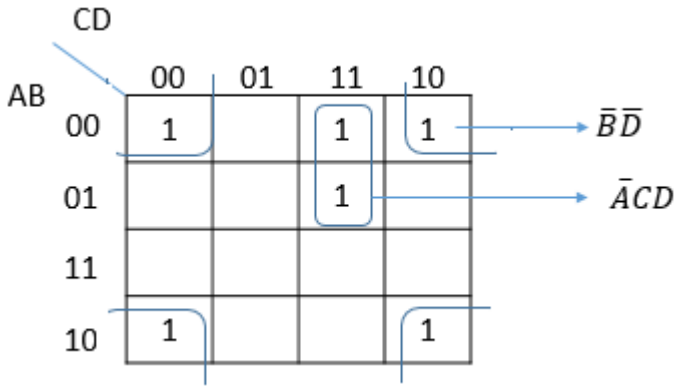
3. Write the canonical expression for the following function $F = \bar{B}\bar{C}\bar{D} + \bar{B}C\bar{D} + \bar{A}CD$ Write the truth table of the function and reduce the function to a three minterms function using a 4-variable K-Map. [10]

Mark distribution [3 + 2 + 5]

$F = \bar{B}\bar{C}\bar{D}(A + \bar{A}) + \bar{B}C\bar{D}\ (A + \bar{A}) + \bar{A}CD(B + \bar{B})$

$A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}\ +\ A\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BCD + \bar{A}\bar{B}CD$

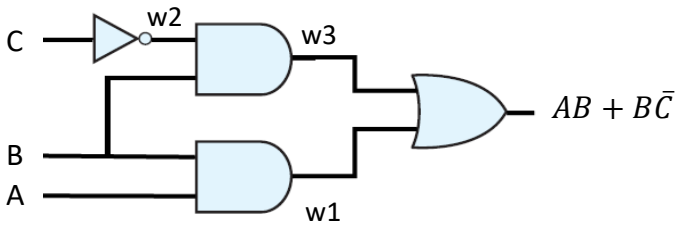
A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



$$F = \bar{A}CD + \bar{B}\bar{D}$$

This is the most simplified form.

If it is written to three minterms form, multiply first term with $(B + \bar{B})$ or second term with either $(A + \bar{A})$ or $(C + \bar{C})$ and apply distributive law.

4.	a.	Develop a Verilog HDL code for the following logic diagram.
		 
		
		module logic_circit(Y,A,B,C);
		output Y;
		input A,B,C;
		wire w1,w2, w3;
		and G1(w1,A,B);
		not G2(w2,C)
		and G3(w3,w2,B);
		or G4(Y,w1,w3);
		endmodule
			[5]

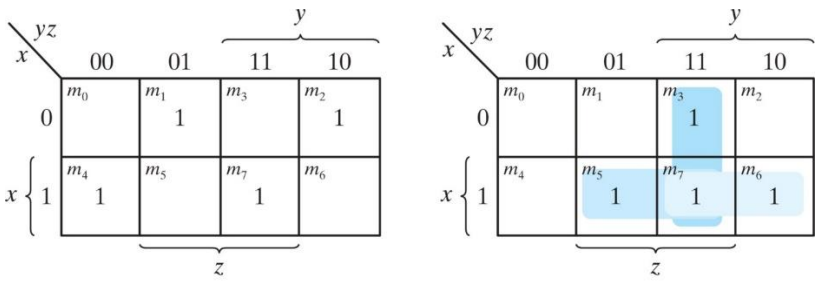
	b.	Find and correct the syntax errors in the following structural level abstraction of Verilog HDL code.
		Errors
		module 1simple_circit(A,B,C,D); //module name cannot start with a number
		output D;
		input A,B,C;
		wire w1,w2;
		and G1(w1,a,b); // port names are case sensitive
		not G2(w2,c) // port names are case sensitive and ; missing (2 Errors)
		or G3(D,w1,w2);
		endmodule; // wrong syntax
		Corrected
		module simple_circit(A,B,C,D);
		output D;
		input A,B,C;
		wire w1,w2;
		and G1(w1,A,B);
		not G2(w2,C);
		or G3(D,w1,w2);
		endmodule	

5.		Design a combinational circuit which will provide sum of three bit binary numbers using following steps. i) Write down the true table of the circuit. [2]	[10]

Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

ii) Make the simplified Boolean function of the circuit. [3]



(a) $S = x'y'z + x'yz' + xy'z' + xyz$ (b) $C = xy + xz + yz$

Sum = XY'Z' + X'Y'Z + XYZ + X'YZ'

= Z(X'Y' + XY) +Z'(XY' + X'Y)

= Z(X⊕Y)' + z'(X⊕Y)

= X ⊕ Y ⊕ Z

Carry = XY + YZ + XZ

= XY + (Y+X)Z

= XY + (Y+ Y'X)Z

= XY + YZ + Y'XZ

= (X+Z)Y + Y'XZ

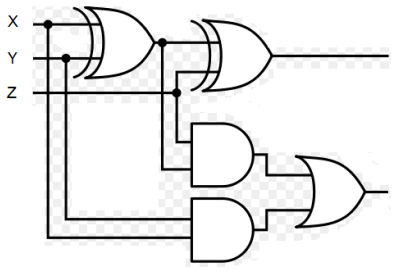
=(X+X'Z)Y + Y'XZ

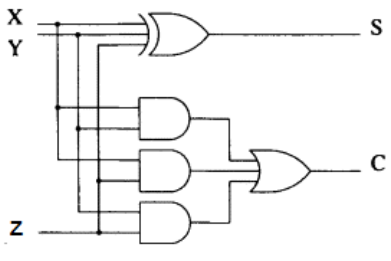
= XY + X'YZ + XY'Z

=XY + (X'Y + XY')Z

=XY+(X⊕Y)Z

iii) Draw the logical diagram of the circuit. [2]





iv) Write the Verilog HDL code of the logical diagram. [3]

```
module fa_gate_level(s,c,x,y,z);
  input x,y,z;
  output s,c;
  wire w1,w2,w3;
  xor xor1(w1,x,y);
  xor xor2(s,w1,z);
  and A1(w2,w1,z);
  and A2(w3,x,y);
  or O1(c,w2,w3);
endmodule
```

Or

```
module fa_gate_level(s,c,x,y,z);
  input x,y,z;
  output s,c;
  wire w1,w2,w3;
  xor xor1(s,x,y,z);
  and A1(w1, x,y);
  and A2(w2,x,z);
 and A3(w3,y,z);
  or O1(c, w1,w2,w3);
endmodule
```

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