VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Fall Semester 2022-2023

Continuous Assessment Test – I

Programme Name & Branch : BTECH CSE **SLOT: D1+TD1**

Course Name & code: Digital Systems Design BECE102L

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

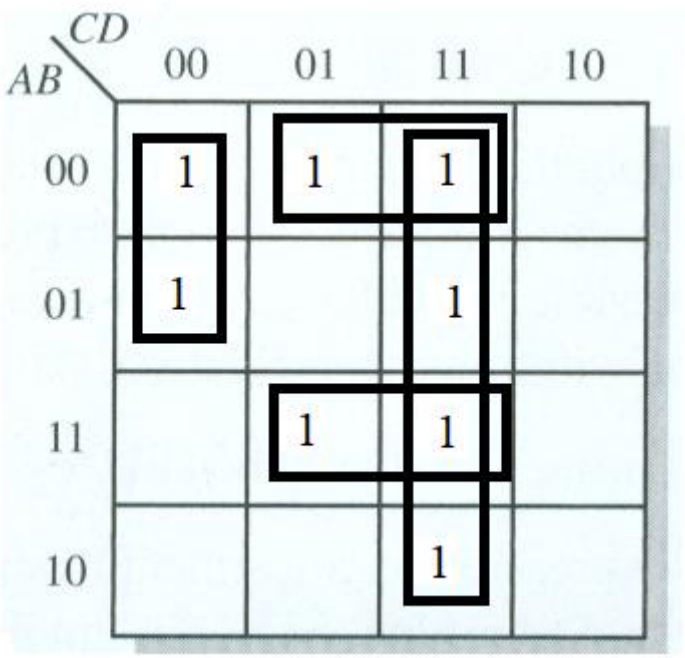
Mention the question number outside the margin clearly. Answer in sequential order with clarity. Draw the diagrams neatly using appropriate pencil and scale.

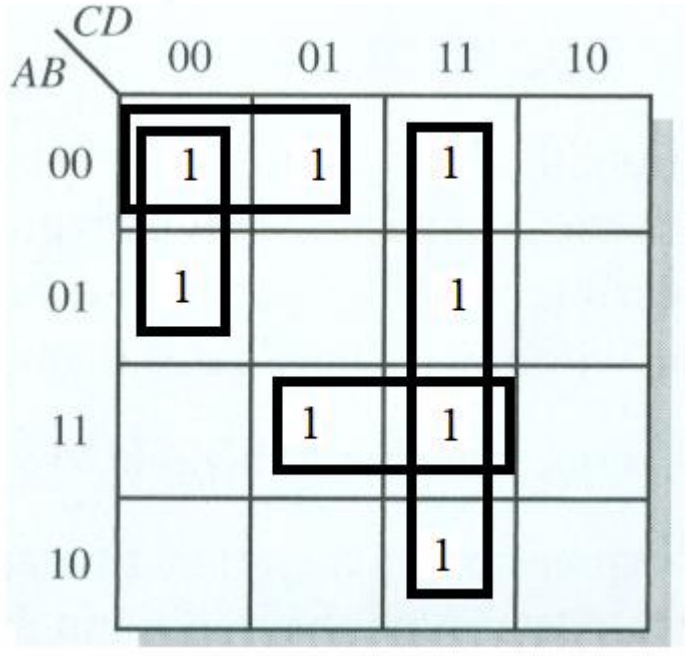
Q.No.	Questions	Max Marks
1.	Simplify the Boolean expression using theorems and postulates. Draw the logic diagram using logic gates for the simplified Boolean expression	
	a) $Y = A'B + B'C + C + A'B'C'D' + C'D'$	5
	$= A'B + (B' + 1)C + (A'B' + 1)C'D'$	
	$= A'B + C + C'D'$	
	$= A'B + (C + C')(C + D')$	
	$= A'B + C + D'$	5
	b) $F(a, b, c, d) = \sum m(0, 1, 3, 8, 9, 13, 15)$	
	F = a'b'c'd' + a'b'c'd + a'b'cd + ab'c'd' + ab'c'd + abc'd + abcd	
	= a'b'c'd' + a'b'c'd + a'b'cd + ab'c'd' + ab'c'd + abc'd + abcd	
	= a'b'c'(d'+d) +ab'c'(d'+d) + a'b'd(c'+c) + abd(c+c')	
	= a'b'c' + ab'c' + a'b'd + abd = b'c'(a'+a) + a'b'd + abd	
	F = b'c' + a'b'd + abd	

2.	a. Explain with an example how digital gates are implemented using CMOS technology.
	
	b. Find the syntax errors in the following declarations (note that names for primitive gates are optional):
	
	module module Exmpl-3(A, B, C, D, F) // Line 1
	inputs A, B, C, Output D, F, // Line 2
	output B // Line 3
	and g1(A, B, D); // Line 4
	not (D, A, C), // Line 5
	OR (F, B; C); // Line 6
	endmodule // Line 7
	
	Line 1: Dash not allowed character in identifier; use underscore: Exmpl_3. Terminate line with semicolon (;).
	Line 2: **inputs** should be **input** (no s at the end). Change last comma (,) to semicolon (;). *Output* is declared but does not appear in the port list, and should be followed by a comma if it is intended to be in the list of inputs. If *Output* is a mispelling of **output** and is to declare output ports, *C* should be followed by a semicolon (;) and *F* should be followed by a semicolon (;).
	Line 3: *B* cannot be declared both as an input (Line 2) and output (Line 3). Terminate the line with a semicolon (;).
	Line 4: *A* cannot be an output of the primitive if it is an input to the module
	Line 5: Too many entries for the not gate (may have only a single input, and a single output). Termiante the line with a semicolon, not a comma.
	Line 6: OR must be in lowercase: change to "or". Replace semicolon by a comma (B,) in the list of ports.
	PS: If student answer any five syntax error, 5 marks can be awarded
		5
		
		5

3.	Use K-maps to find the minimum-cost SOP and POS expressions for the function and draw the corresponding logic diagrams of SOP and POS expressions $F(a,b,c,d) = a'c'd' + cd + a'b'd + abc'd$ Truth Table a b c d F 0 0 0 0 1 0 0 0 1 1 0 0 1 0 0 0 0 1 1 1 0 1 0 0 1 0 1 0 1 0 0 1 1 0 0 0 1 1 1 1 1 0 0 0 0 1 0 0 1 0 1 0 1 0 0 1 0 1 1 1	**10**

1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1



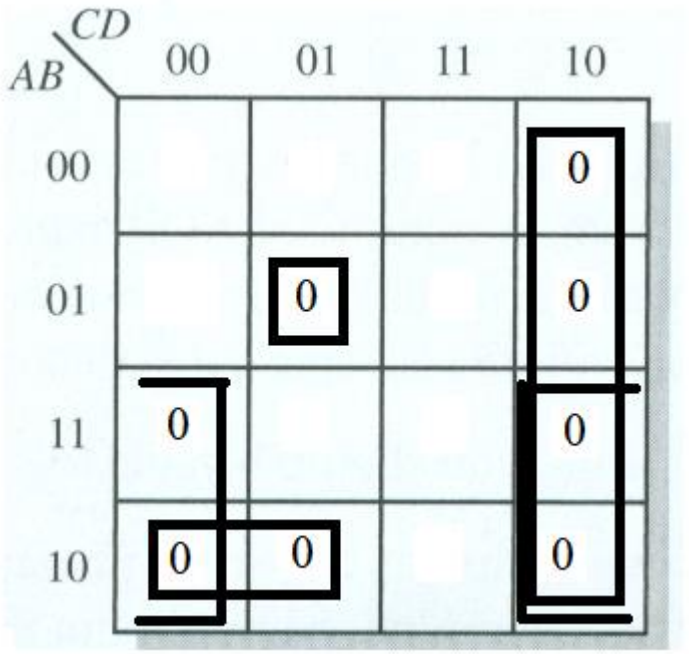


SOP

F = A'C'D' + A'B'D + ABD + CD

(OR)

F = A'C'D' + A'B'C' + ABD + CD



POS

F' = CD' + AD' + AB'C' + A'BC'D

F = (C'+D)(A'+D)(A'+B+C)(A+B'+C+D')

4. Design a combinational circuit with three inputs and one output. Draw the corresponding truth table and Logic diagrams. **5**

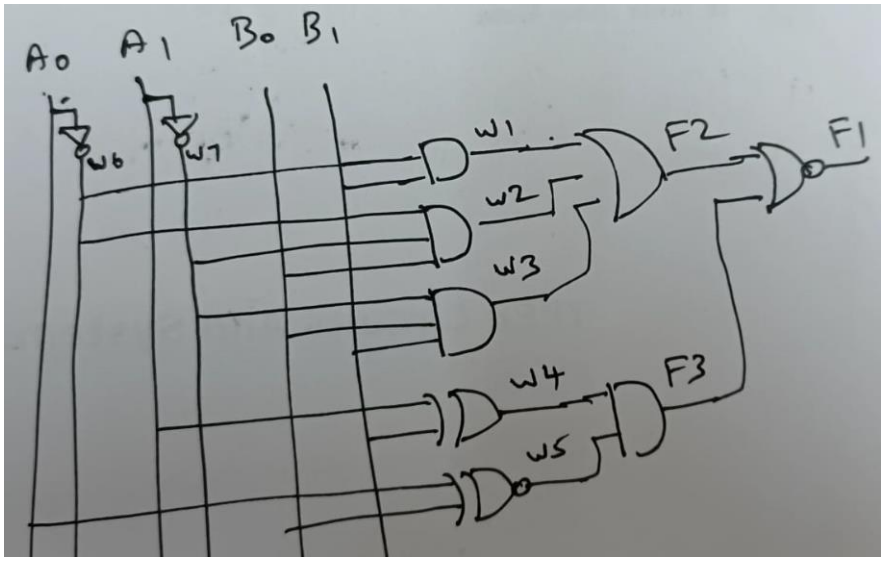
(a) The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.

a	b	c	y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

y = a'b' + a'c'

(b) The output is 1 when the binary value of the inputs is an even number. **5**

a	b	c	y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

	y = c'	
5.	Draw the truth table and logic diagram of the digital circuit specified by the following Verilog description: **module** Circuit_B (F1, F2, F3, A0, A1, B0, B1); **output** F1, F2, F3; **input** A0, A1, B0, B1; **nor** (F1, F2, F3); **or** (F2, w1, w2, w3); **and** (F3, w4, w5); **and** (w1, w6, B1); **or** (w2, w6, w7, B0); **and** (w3, w7, B0, B1); **not** (w6, A1); **not** (w7, A0); **xor** (w4, A1, B1); **xnor** (w5, A0, B0); **endmodule**  #A0A1B0B1F1F2F3 # 0 0 0 0 0 1 0 # 0 0 0 1 0 1 0 # 0 0 1 0 0 1 1 # 0 0 1 1 0 1 0 # 0 1 0 0 0 1 0 # 0 1 0 1 0 1 1 # 0 1 1 0 0 1 0 # 0 1 1 1 0 1 0	**10**

	# 0 0 0 0 0 1 0 # 0 0 0 1 0 1 0 # 0 0 1 0 0 1 1 # 0 0 1 1 0 1 0 # 0 1 0 0 0 1 0 # 0 1 0 1 0 1 1 # 0 1 1 0 0 1 0 # 0 1 1 1 0 1 0 # 1 0 0 0 0 1 0 # 1 0 0 1 0 1 0 # 1 0 1 0 0 1 0 # 1 0 1 1 0 1 0 # 1 1 0 0 0 1 1 # 1 1 0 1 1 0 0 # 1 1 1 0 1 0 0 # 1 1 1 1 0 1 1	