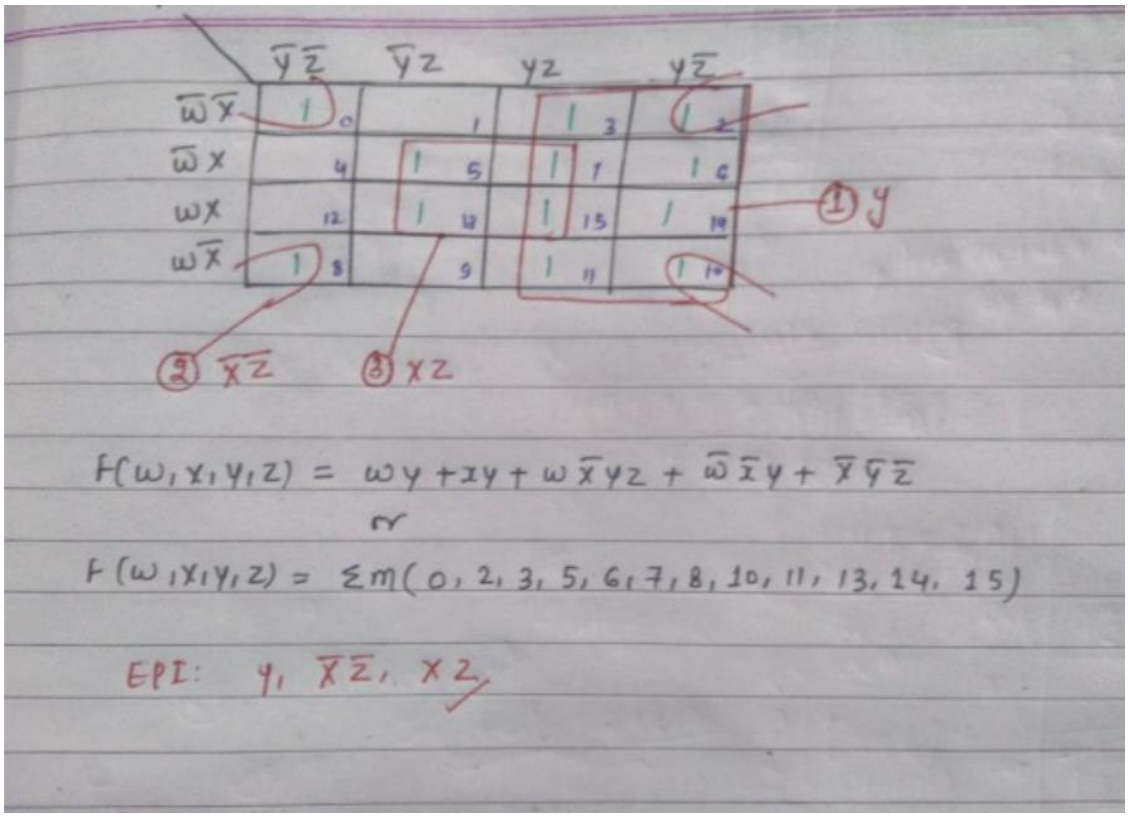
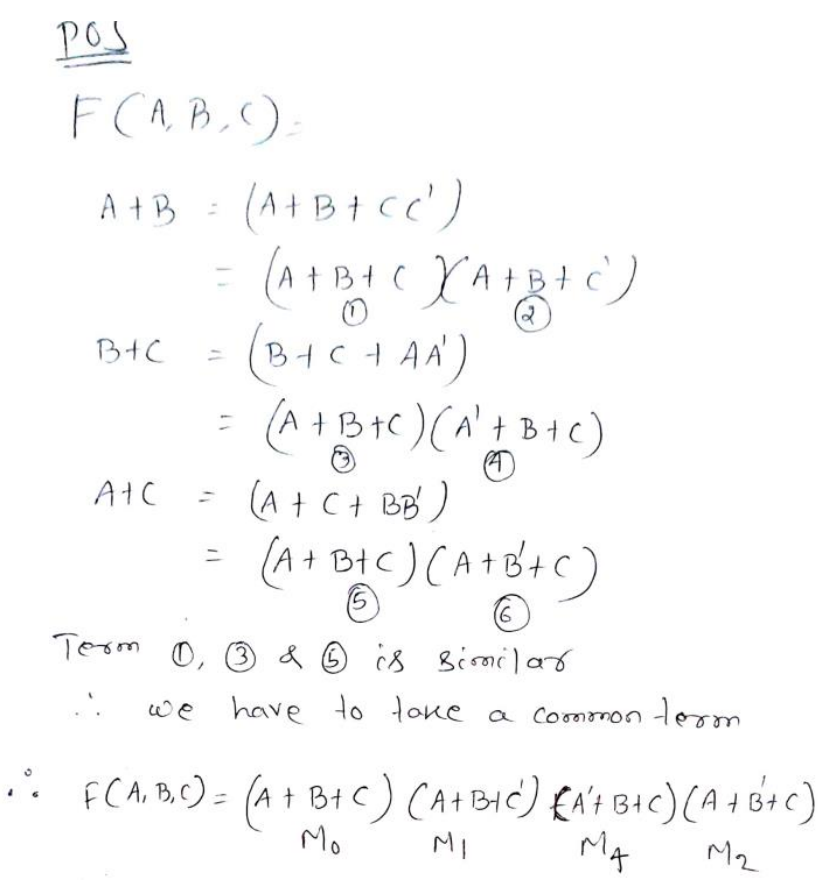
SCHOOL OF ELECTRONICS ENGINEERING
Fall Semester 2022-2023
CAT- I

Course: BECE102L - Digital Systems Design **B. Tech (ECE)**
Slot: F2+TF2 **Max. Marks: 50**
Date: 3/09/2022 **Time: 3:00 PM to 4:30 PM**
Class Id- VL2022230102860, VL2022230102863, VL2022230102865, VL2022230102867, VL2022230102868, VL2022230102870, VL2022230102872, VL2022230102874, VL2022230102876, VL2022230102878.

Answer all the Question

Q. No.	Question	Max. marks
1.	i. Consider the Boolean function, $F(w,x,y,z) = wy + xy + w'xyz + w'x'y + xz + x'y'z'$. Simplify using K-map and identify the complete set of essential prime implicants? **Ans-**  ii. Simplify the following Boolean expression using Boolean algebra. *a.* $A'B(D' + C'D) + B(A + A'CD)$ (to one literal) Ans- *A'B(D' + C'D) + B(A + A'CD) = B(A'D' + A'C'D + A + A'CD)* *= B(A'D' + A + A'D(C + C') = B(A + A'(D' + D)) = B(A + A') = B* b. *BC'D' + ABC' + AC'D + AB'D + A'BD'* (to three literals) Ans- [A'BD'+ABC'+BC'D']+[ABC'+AB'D+AC'D] Rearrange and add another ABC' term	i.5 ii.2.5 +2.5

	[A'(BD')+A(BC')+(BD')(BC')]+[(AC')B+(AD)B'+(AC')(AD)] Group concensus A'BD'+ABC'+ABC'+AB'D Drop duplicate term A'BD'+ABC'+AB'D	
2.	i. Convert the given expression in SOP and POS canonical form $F(A,B,C) = (A+B)(B+C)(A+C)$ **Ans-**  	i.5 ii.5

SOP :

$F(A,B,C) = (A+B)(B+C)(A+C)$

$f(A,B,C) = \pi(3, 5, 6, 7) = M_3\ M_5\ M_6\ M_7$

$= (A'+B'+C')(A'+B+C')(A'+B'+C)(A'+B'+C')$

Applying De Morgan's theorem,

$= \overline{M_3 M_5 M_6 M_7}$

$= \overline{M_3} + \overline{M_5} + \overline{M_6} + \overline{M_7}$

$= A'BC + AB'C + ABC' + ABC$

$= m_3 + m_5 + m_6 + m_7 = \Sigma m\,(3, 5, 6, 7)$

$M_j' = m_j$

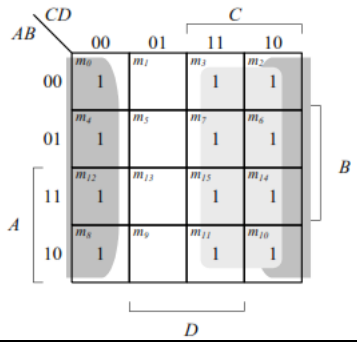
M = Maxterm

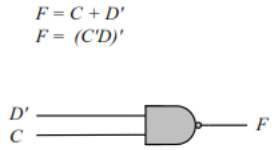
m = minterm

j = 0, 1, 2 ... $2^n - 1$

ii. Simplify the following using K-Map and draw the logic diagram using only NAND gates.
F(*a,b,c,d*) =$ac'd' + a'c + abc + ab'c + a'c'd'$

Ans-





3.

i. Write the expansion results for the given formats.

Format	Expansions
//let x = 4'b1010	**&x**?
//let x = 4'b1010, y = 4'b0000	**x | y**?
// let x = 4'b1100 **y = x << 2;**	**y**=?
//let a = 1'b1, b = 2'b00, c = 2'b10, d = 3'b110 **y = {a, b, c, d, 3'b001}**	**y**=?
//let a = 1'b1, b = 2'b00, c = 2'b10, d = 3'b110 **y = { 4{a}, 2{b}, c }**	**y**=?

i.5
ii.5

Ans

Format	Expansions
//let x = 4'b1010	// **&x** //equivalent to **1 & 0 & 1 & 0.** Results in **1'b0**
//let x = 4'b1010, y = 4'b0000 x | y	//bitwise OR, result is 4'b1010

// let x = 4'b1100
y = x << 2;
	// y is 4'b0000

//let a = 1'b1, b = 2'b00, c = 2'b10, d = 3'b110
y = {a, b, c, d, 3'b001}
	y is then 11'b10010110001

//let a = 1'b1, b = 2'b00, c = 2'b10, d = 3'b110 y = { 4{a}, 2{b}, c }	y = 8'b1111000010

ii. Implement the following multiple output Boolean functions $F_1(A,B,C)=\Sigma m(0,4,7)+ \Sigma dm(2,3)$, $F_2(A,B,C)= \Sigma m(1,5,6)$ and $F_3(A,B,C)= \Sigma m(0,2,4,6)$ with suitable decoder and external gates. What is the advantage of decoder.

Ans-

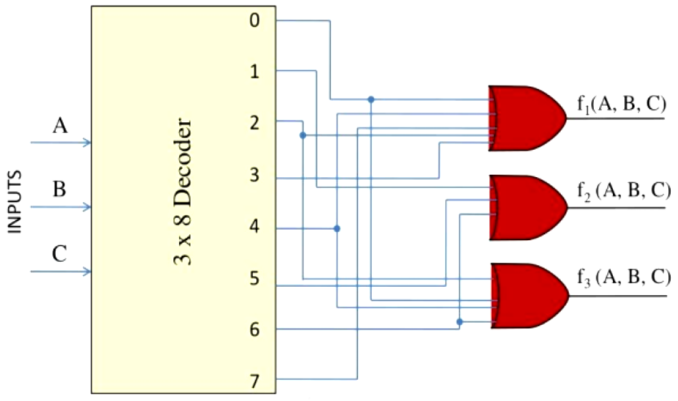
Implement the following multiple output Boolean functions with suitable decoder and external gates. What is the advantage of the decoder?

$f_1(A, B, C) = \sum m(0,4,7)+ d(2,3)$

$f_2(A, B, C) = \sum m(1,5,6)$

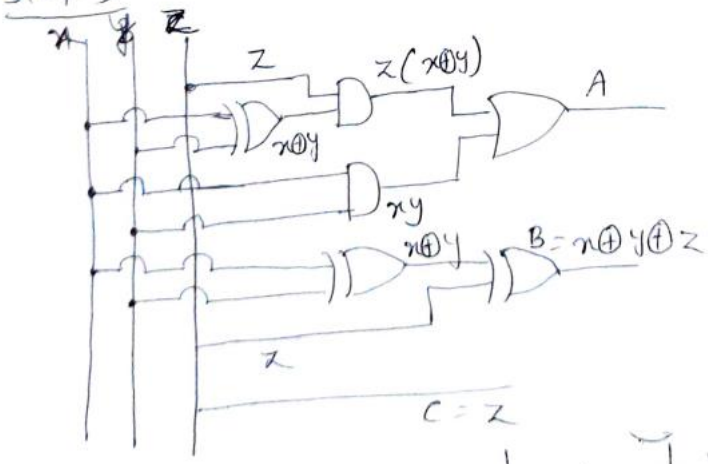
$f_3(A, B, C) = \sum m(0,2,4,6)$

Solution: f1 consists of don't care conditions. So we consider them to be logic 1.



A decoder is a device that generates the original signal as output from the coded input signal and converts n lines of input into 2^n lines of output. An AND gate can be used as the basic decoding element because it produces a high output only when all inputs are high

4.	Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Write the Verilog code using data flow modelling for the designed circuit.	10

	Ans-
	# 3 inputs x, y, z and 3 outputs A, B, C.
	#Step 1
	#Step 2
	A = x'yz + xy'z + xyz' + xyz
	= x(y'z + yz') + yz(x + x')
	= x(y ⊕ z) + yz
	or,
	= z(x'y + xy') + xy(z + z')
	= z(x ⊕ y) + xy
	B = x'y'z + x'yz' + xy'z' + xyz
	= x'(y'z + yz') + x(y'z' + yz) ; Let's k = y ⊕ z, ∴ k' = y ⊕ z'
	= x'k + xk'
	= x ⊕ k = x ⊕ y ⊕ z
	C = x'y'z' + x'yz' + xy'z' + xyz'
	= x'z'(y + y') + xz'(y + y')
	= x'z' + xz' = z'(x + x')
	= z
	Step-3
	 
	
	#1. write the verilog code in dataflow modeling.	

5.	Write Verilog code for the following logic diagram shown in Figure.1 using structural modelling. Consider A as addend and B as augend.	10

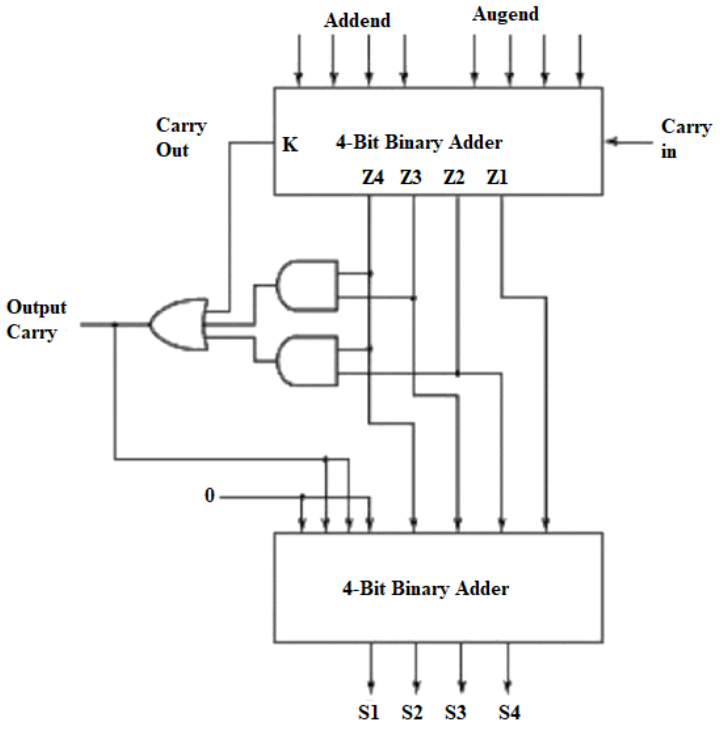


Figure.1

Ans-Referral code for 4-bit adder and along with this code two AND gate and one OR gate can be attached for Output Carry.

```
// Module to implement a 4-bit adder
// Structural description using fa module

module  adder4(sum, co, a, b, ci) ;
        output   [3:0] sum ;
        output   co ;
        input    [3:0] a ;
        input    [3:0] b ;
        input    ci ;
        wire     [3:1] c ;

        fa  g0(sum[0], c[1], a[0], b[0], ci) ;
        fa  g1(sum[1], c[2], a[1], b[1], c[1]) ;
        fa  g2(sum[2], c[3], a[2], b[2], c[2]) ;
        fa  g3(sum[3], co, a[3], b[3], c[3]) ;

endmodule
```