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SCHOOL OF ELECTRONICS ENGINEERING

CONTINUOUS ASSESSMENT TEST II, WINTER 2022-23

BECE102L- Digital Systems Design

Time: 1.30 Hrs. Slot: C2+TC2 Max. Marks: 50

Faculty(s): Anand S, George Jacob, Hemanta Kumar Sahu

Answer All Questions

1. A digital circuit has three inputs (a, b, and c) and one output (y). When a = 0, y is equal to the XOR of b and c, and when a = 1, y is the XNOR of b and c. Write a behavioural-level Verilog programme to implement the logic. Also, write a suitable test bench. Provide line-by-line comments. [10]

```
module cat2(y,a,b,c);
 input a,b,c;
 output y;
 reg y;
 always@(*)
 begin
  if (a==1'b0)
    y=b^c;
  else if(a==1'b1)
    y=b~^c;
  end
 endmodule

 module cat2_tb;
  reg a,b,c;
  wire y;
  integer i;
  cat2 init(y,a,b,c);
  initial
  begin
    for(i=1'b0; i<8; i=i+1)
      begin
      {a,b,c}=i;
      #5;
    end
  $stop;
  end
endmodule
```

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

2. In a communication system, data is transmitted in the form of unique 3-bit words that are generated using a digital system that has 8 input lines. These 3-bit words are generated based on the inputs received by the communication system. Suggest a digital system that will be capable of this conversion. Draw the truth table of this system, design the circuit, and draw the logic circuit. [10]

Encoder can be used for this conversion
The encoder has 2^n input lines and n output lines

Expression for each output

$x = D_4+D_5+D_6+D_7$

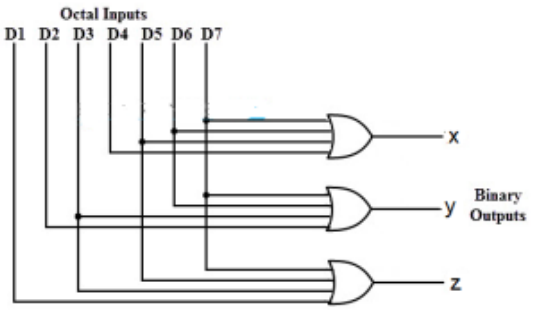
$y = D_2+D_3+D_6+D_7$

$z = D_1+D_3+D_5+D_7$

Truth Table

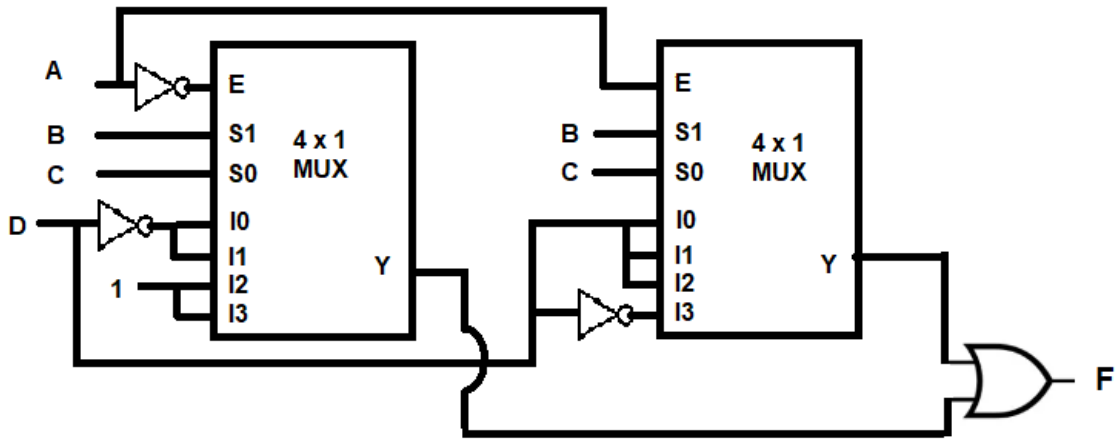
Inputs								Outputs		
D0	D1	D2	D3	D4	D5	D6	D7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Digital Circuit Diagram



3. Implement the following Boolean function using two 4×1 multiplexers. F(A,B,C,D) = Σ(0,2,4,5,6, 7,9,11,13,14). Create the truth table and draw the circuit implementation using multiplexers. [10]

A	B	C	D	F	
0	0	0	0	1	F=D’
0	0	0	1	0	
0	0	1	0	1	F=D’
0	0	1	1	0	
0	1	0	0	1	F=1
0	1	0	1	1	
0	1	1	0	1	F=1
0	1	1	1	1	
1	0	0	0	0	F=D
1	0	0	1	1	
1	0	1	0	0	F=D
1	0	1	1	1	
1	1	0	0	0	F=D
1	1	0	1	1	
1	1	1	0	1	F=D’
1	1	1	1	0	



4. Implement the binary equivalent multiplication of two-signed numbers with the necessary steps. (+6 × -3). Identify the suitable method and explain the step-by-step procedure to implement it. [10]

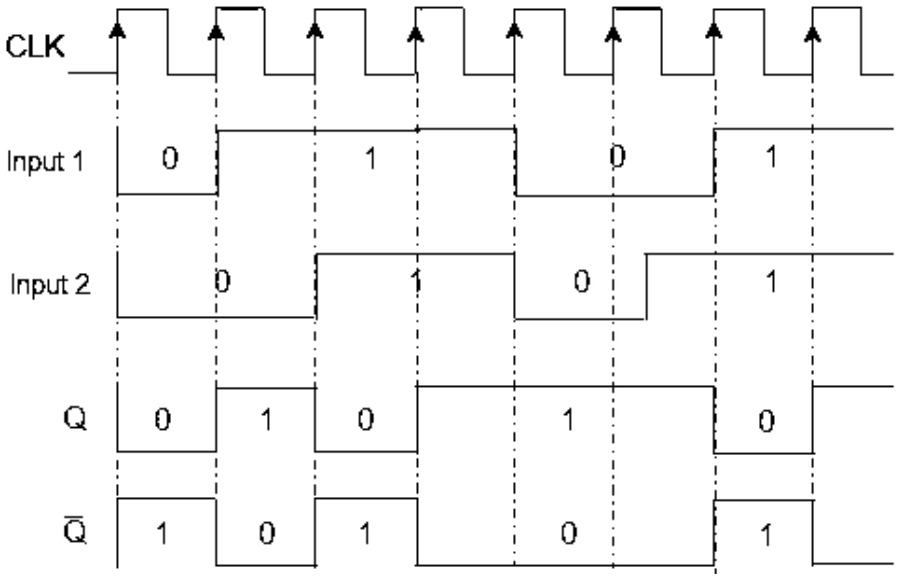
Multiplication 0101 x 0100 (6x-3)

A = 0000 Q = 1101 M = 0110 Q_{-1} = 0 Count = 4 (Number of bits)

Count	A				Q				Q_{-1}	Action	
	A_3	A_2	A_1	A_0	Q_3	Q_2	Q_1	Q_0			
	0	0	0	0	1	1	0	1	0	Check code of Q_0 Q_{-1}	10
4	1	0	1	0	1	1	0	1	0	A = A-M 0000 – 0110 = 0000 + 0011 (2's comp)	0000 1010+ 1010
	1	1	0	1	0	1	1	0	1	ARS	
	1	1	0	1	0	1	1	0	1	Check code of Q_0 Q_{-1}	01
3	0	0	1	1	0	1	1	0	1	A=A+M	1101 0110+ 10011
	0	0	0	1	1	0	1	1	0	ARS	
	0	0	0	1	1	0	1	1	0	Check code of Q_0 Q_{-1}	10
2	1	0	1	1	1	0	1	1	0	A = A-M	0001 1010+ 1011
	1	1	0	1	1	1	0	1	1	ARS	
1	1	1	0	1	1	1	0	1	1	Check code of Q_0 Q_{-1}	11
	1	1	1	0	1	1	1	0	1	ARS	
0	1	1	1	0	1	1	1	0		Stop	

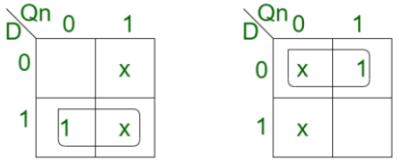
0110 x 1101 = 1110 1110

5. Identify the flip-flop and write its characteristic table and equation from the following timing diagram. Convert it into a D flip-flop. Explain the procedure for a flip-flop conversation in details. [10]



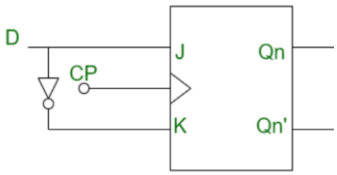
The given flip-flop is J K Flip-flop.

D	Qn	Qn+1	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0



J = D

J = D’



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