



School of Computer Engineering
FS_2022-23 (CAT-II)

Course Code : BECE102L

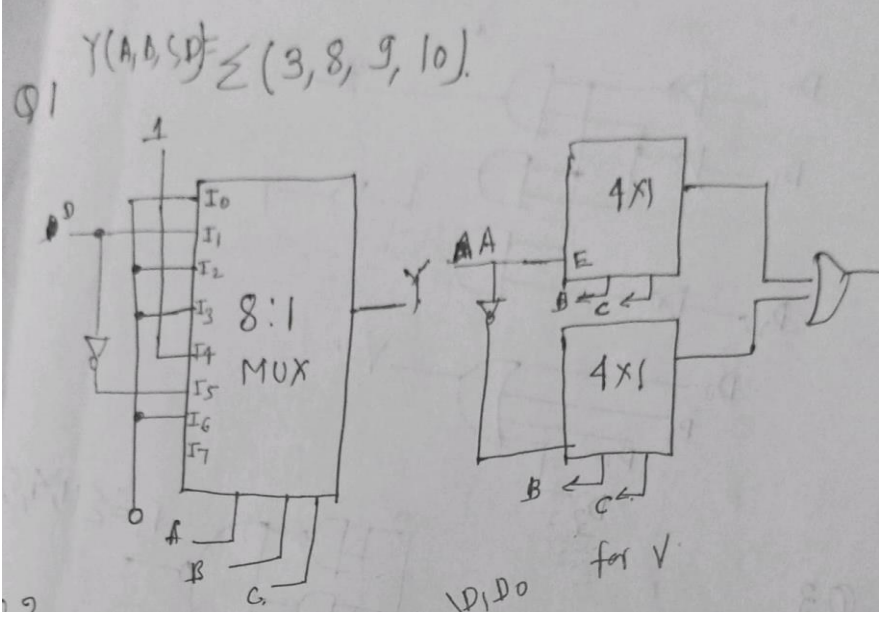
Duration : 90 Minutes.

Course Name : Digital Systems Design

Faculty Name : SHWETA B THOMAS, ABRAHAM SAMPSON S, ABDUL MAJEED K K, MANIKANDAN SP, ANTONY XAVIER GLITTAS X, JAYANANDAN T, CHITTARANJAN NAYAK, VIKAS VIJAYVARGIYA, NAVEES AHMED S, ANILKUMAR P

Slot : D2+TD2

Max. Marks : 50M

S. No	Course Outcomes (CO's) Mapping (CO1-CO6)	Marks Allotted
Q 1	<p>(i) Implement the following Boolean function (Y) with an 8 × 1 multiplexer and external NAND gates.</p> <p>$Y(A, B, C, D) = \prod M(0, 1, 2, 4, 5, 6, 7, 11, 12, 13, 15)$</p> <p>(ii) Realize the function in part (i) using 4 × 1 multiplexer</p> 	10
Q 2	<p>(i) Design a combinational circuit with inputs D0, D1, D2, D3 and outputs X, Y, V. The operation of the combinational circuit is such that if two or more inputs are equal to 1 at the same time, highest priority input is considered. The order of priority is D0>D1>D2>D3. Here V is the valid bit indicator that is set to 1 when one or more inputs are equal to 1.</p>	10

(ii) Write only a test bench in Verilog to verify the design circuit in part (i). Here consider module name is "Priority_Circuit" and inputs D0, D1, D2, D3 and outputs X, Y, V.

Q2.

inputs				outputs		
D ₃	D ₂	D ₁	D ₀	X	Y	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

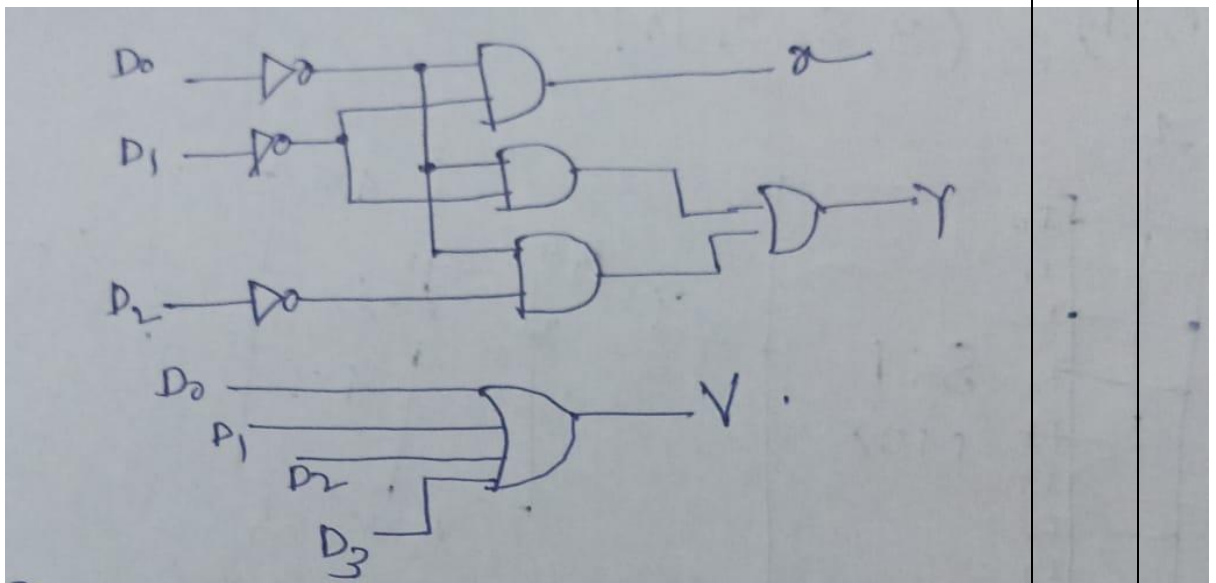
D ₃ D ₂	D ₁ D ₀	for V			
		00	01	11	10
00			1	1	1
01		1	1		1
11		1	1	1	1
10		1	1	1	1

D ₃ D ₂	D ₁ D ₀	for X			
		00	01	11	10
00		X			
01		1			
11		1			
10		1			

$$X = D_1 D_0$$

D ₃ D ₂	D ₁ D ₀	for Y			
		00	01	11	10
00		X			1
01					1
11					1
10		1			1

$$Y = D_0 D_2 + D_1 D_0$$

$$V = D_0 + D_1 + D_2 + D_3$$


Q The outputs of a combinational circuit are defined by the following three Boolean functions:

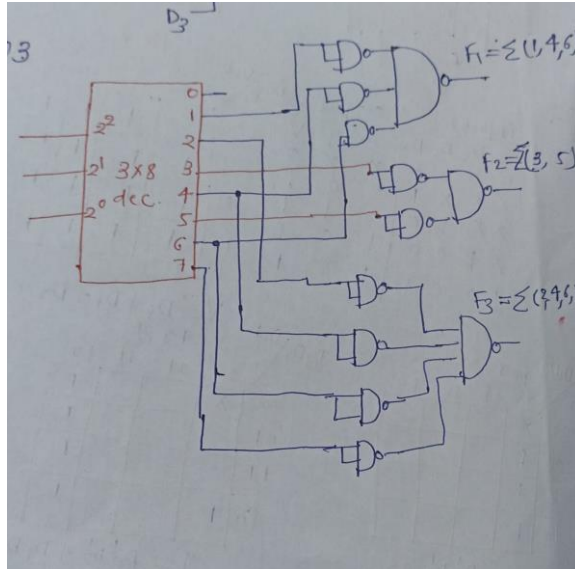
3 $F_1(A, B, C) = \sum(1, 4, 6)$

$F_2(A, B, C) = \sum(3, 5)$

$F_3(A, B, C) = \sum(2, 4, 6, 7)$

Implement the circuit using 3x8 decoder and NAND gates only.

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Q A New clocked X-Y flip-flop is defined with two inputs, X and Y in addition to the clocked input. The flip flop functions as follows:

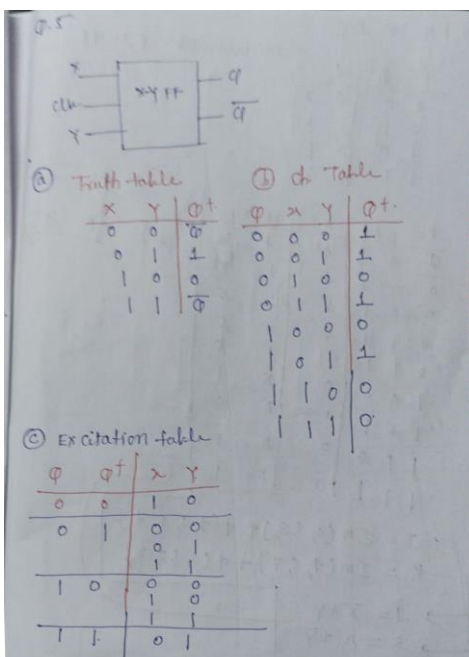
If XY=01, the flip flop state (Q) becomes 1 at the next clock pulse

If XY=10, the flip flop state (Q) becomes 0 at the next clock pulse.

If X=Y, the flip flop toggles its state (Q) at the next clock pulse.

- i. Provide the truth table for the X-Y flip flop
- ii. Provide the characteristics table
- iii. Provide the Excitation table for the X-Y flip flop
- iv. Implement X-Y flip flop using a J-K flip flop

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③ JK to X-Y. \Rightarrow excitation table + JK FF.

ϕ	ϕ'	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

P.S	ϕ	ϕ'	N.S	FF	FF'
Q	X	Y	ϕ'	J	K
0	0	0	1	1	X
0	0	1	1	1	X
0	1	0	0	0	X
0	1	1	1	1	X
1	0	0	0	X	1
1	0	1	1	X	0
1	1	0	0	X	1
1	1	1	1	X	1

$J = \sum m(0, 1, 3) + d(4, 5, 6, 7)$
 $K = \sum m(4, 6, 7) + d(0, 1, 3)$
 $J = \bar{X} + Y$
 $K = X + \bar{Y}$

Q 5 Obtain the Boolean expressions ($A > B$, $A = B$ and $A < B$) for 6-bit magnitude comparator and then after model the expression using data flow modelling.

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$A = A_5 A_4 A_3 A_2 A_1 A_0$
 $B = B_5 B_4 B_3 B_2 B_1 B_0$
 $A_i = B_i \Rightarrow x_i = A_i B_i + \bar{A}_i \bar{B}_i$
 $\therefore A = B \Rightarrow x_5 x_4 x_3 x_2 x_1 x_0$
 $A < B \Rightarrow \bar{A}_5 B_5 + x_5 \bar{A}_4 B_4 + x_5 x_4 \bar{A}_3 B_3 + x_5 x_4 x_3 \bar{A}_2 B_2 + x_5 x_4 x_3 x_2 \bar{A}_1 B_1 + x_5 x_4 x_3 x_2 x_1 \bar{A}_0 B_0$
 $A > B \Rightarrow A_5 \bar{B}_5 + x_5 A_4 \bar{B}_4 + x_5 x_4 A_3 \bar{B}_3 + x_5 x_4 x_3 A_2 \bar{B}_2 + x_5 x_4 x_3 x_2 A_1 \bar{B}_1 + x_5 x_4 x_3 x_2 x_1 A_0 \bar{B}_0$