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Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING (SENSE)

Continuous Assessment Test – I
Winter Semester -2022-23

Programme Name & Branch : B.Tech ECE
Course Name & Code : BECE204L- Microprocessors and Microcontrollers

Slot: C1 Answer all the questions Exam Duration:50 Minutes

S.No	Question	Marks	CO	BL
1	(a) Indicate the addressing modes for the following 8051 instructions (i) MOV R0, #56H (ii) MOVC A, @A+DPTR (iii) MOV 38H, R0 (iv) MOV R0, 38H (v) ADD A, @R1 (b) Identify if the following 8051 instruction have any error, if so give the correct instructions (i) MOV @R2, A (ii) DEC DPTR (iii) CPL R3 (iv) AND A, B (v) MUL A,B	5+5	CO3	L3

2	Analyze the following 8051 assembly program and show the stack and stack pointer during the execution of the program. Assume the default stack area.
	MOV R6, #25H
	MOV R1, #12
	MOV R4, #0F3H
	PUSH 6
	PUSH 1
	PUSH 4
	POP 7
	POP 5
	POP 3
	END
		10	CO3	L4

3	Assume that 8051 internal RAM locations 40H – 44H have the following values, write an assembly program to find the sum of the values. At the end of the program, register A should contain the low byte and R7 the high byte of the sum. 40H = (7DH) 41H = (EBH) 42H = (C5H) 43H = (5BH) 44H = (30H)	10	CO3	L6

<table>
<tr>
<td>4.</td>
<td>(a) Write an 8051 assembly program to generate a waveform with 30% duty cycle on the port pin P1.2.

(b) For the given 8051 assembly program, find out the time required to execute it, if XTAL frequency is 11.0592 MHz.
<table>
<tr><td>MOV R4, #0FH</td><td>1 machine cycle</td></tr>
<tr><td>L1: ADD A, R4</td><td>1 machine cycle</td></tr>
<tr><td>MOV B, #89H</td><td>1 machine cycle</td></tr>
<tr><td>MUL A B</td><td>2 machine cycle</td></tr>
<tr><td>INC A</td><td>1 machine cycle</td></tr>
<tr><td>DJNZ R4, L1</td><td>2 machine cycle</td></tr>
</table>
</td>
<td>5+5</td>
<td>CO4</td>
<td>L5</td>
</tr>
<tr>
<td>5.</td>
<td>Assume a switch is connected at port pin P1.4, monitor the status of the switch. If the status of the switch is high then transfer data from Port P0 to P2, else transfer data from Port P0 to P3.</td>
<td>10</td>
<td>CO4</td>
<td>L6</td>
</tr>
</table>

KEY

CAT 1 – ANSWER KEY

1. (a)

i. MOV R0, #36H → Immediate addressing mode

ii. MOVC A, @A+DPTR → Indexed addressing mode

iii. MOV 38H, R0 → Register addressing mode

iv. MOV R0, 38H → Direct addressing mode

v. ADD A, @R1 → Indirect addressing Mode

(b) i. MOV @R2, A → @R2 is not allowed
MOV R2, A & MOV @R0, A

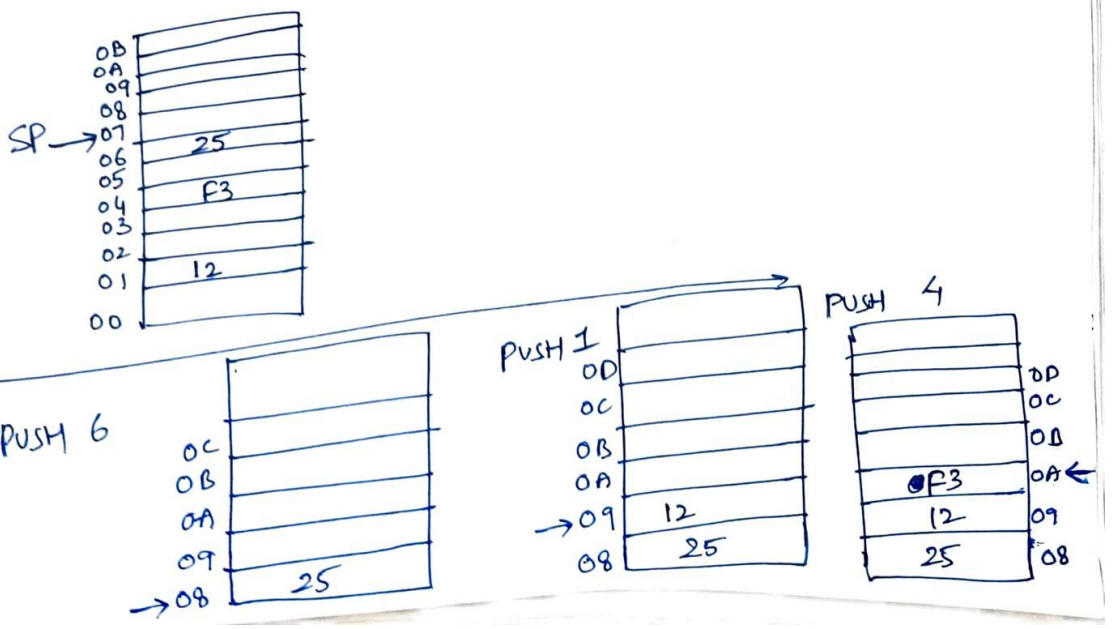
ii. DEC DPTR → Wrong Instructions
only INC DPTR

iii. CPL R3 → Wrong instructions
CPL A

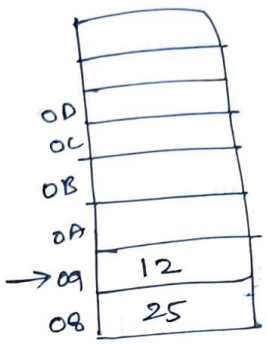
iv. AND A,B → ANL A,B

v. MUL A,B → MUL AB

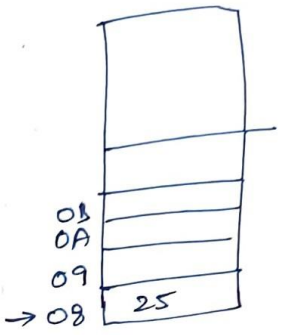
2.



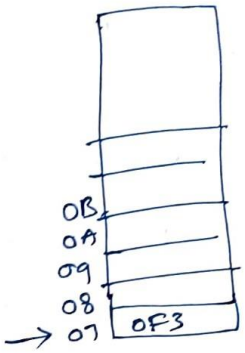
POP 7



POP 5



POP 3



3. Ans.

```
ORG 6000H
MOV A, #00H
ADD A, 40H
JNC L1
INC R7
L1: ADD A, 41H
    JNC L2
    INC R7
L2: ADD A, 42H
    JNC L3
    INC R7
L3: ADD A, 43H
    JNC L4
    INC R7
L4: ADD A, 44H
    JNC L5
    INC R7
L5: NOP
HERE: SJMP HERE
    END
```

4.

$$\frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{3}{10}$$

$T_{ON} = 3\,T_{OFF}$

```
        ORG   0000H
HERE:   SETB  P1.2
        ACALL DELAY
        ACALL DELAY
        ACALL DELAY
        CLR   P1.2
        ACALL DELAY
        ACALL DELAY
        ACALL DELAY
        ACALL DELAY
        ACALL DELAY
        ACALL DELAY
        ACALL DELAY
        SJMP  HERE
DELAY:  MOV   R1, #0FFH
L1:     DJNZ  R1, L1
        RET
        END
```

4b.

```
MOV  R4, #0FH      → 1MC
L1:  ADD A, R4     → 15 X 1MC
     MOV B, #89H   → 15X 1MC
     MUL AB        → 15X 2MC
     INC A         → 15X 1MC
     DJNZ R4, L1   → 15X 2MC
```

$1 + 15(7)$

$= 106$ MC

Delay $= 106 \times 1.085\ \mu sec$

$= 115.01\ \mu sec$

5.

```
        ORG 0000h
        SETB P1.4
HERE:   JNB  P1.4, L1
        MOV  A, P0
        MOV  P2, A
        SJMP HERE
L1:     MOV  A, P0
        MOV  P3, A
        SJMP HERE
        END
```

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