VIT

Vellore Institute of Technology

Continuous Assessment Test – I

Programme Name & Branch: B.Tech, ECE

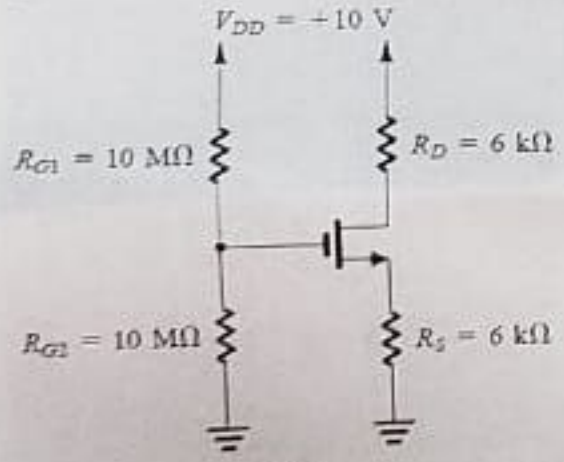
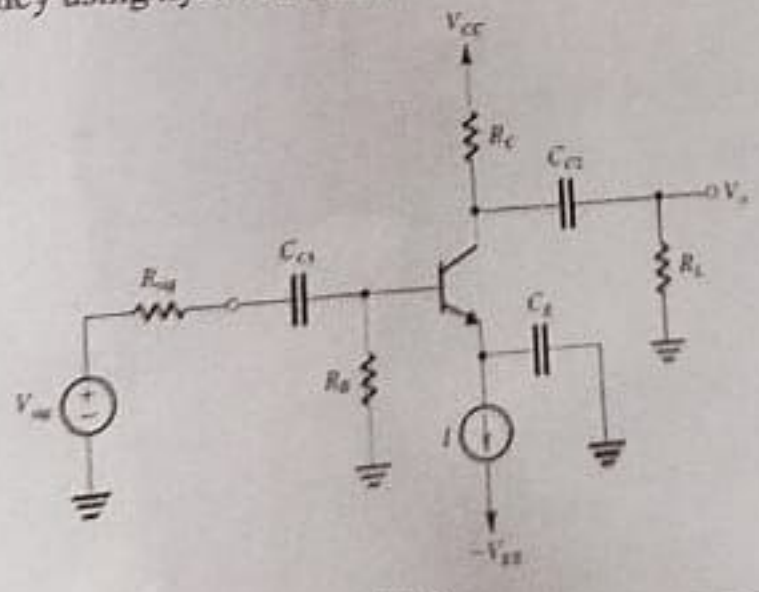
Course Name & Code: Analog Circuits-BECE 206L

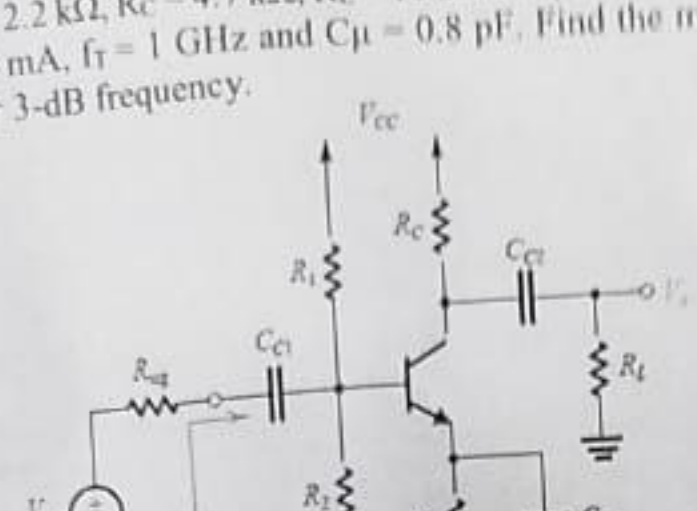
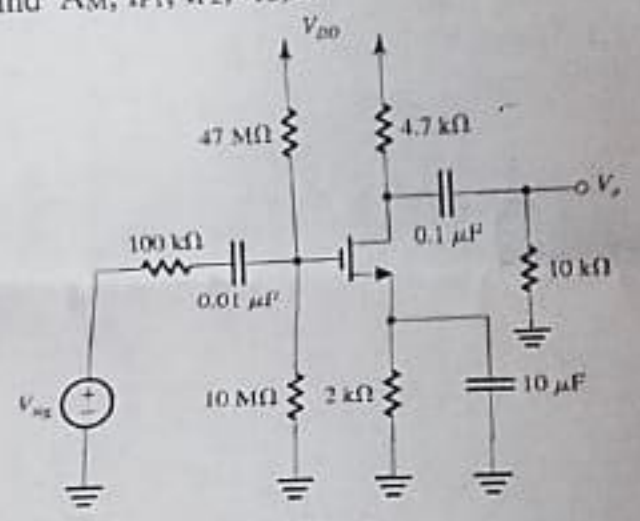
Semester: Fall-2023-24 **Slot:** G1 **Exam Duration:** 90 Min **Maximum Marks:** 50

General instruction(s):

Assume constants whenever it is needed

Answer all Questions

S.No.	Question	Marks	CO	BL
1.	Determine the Q point, DC load line and all the nodal voltages for the circuit shown in Fig.1. Given Vtn = 1V and Kn'(W/L) = 1 mA/V^2.  Fig.1	10	1	L3
2.	Derive the expressions for the mid band gain A_M and the upper 3-dB frequency f_H of the Common Emitter amplifier circuit shown in Fig.2 at high frequency using hybrid π model.  Fig.2	10	1	L3

3.	For the circuit shown in Fig.3, V_{CC} = 5V, Rsig = 10 kΩ, R_1 = 68 kΩ, R_2 = 27 kΩ, R_E = 2.2 kΩ, R_C = 4.7 kΩ, R_L = 10 kΩ and β = 200. The collector current is 0.8 mA, f_T = 1 GHz and C_μ = 0.8 pF. Find the midband gain and the upper 3-dB frequency.  Fig.3	10	1	L3
4.	For the CS amplifier circuit given in Fig.4.The circuit is biased to have g_m=1mA/V. Find A_M, f_{P1}, f_{P2}, f_{P3},f_L.  Fig.4	10	1	L3
5	A class A Power amplifier is designed with V_{DD} = 15 V and R_D = 7 kΩ and Kn'(W/L) = 4 mA/V^2 , V_{TN} = 1 V, and λ = 0. Assume the output voltage swing is limited to the range between the transition point and V_{DS} = 9 V, to minimize nonlinear distortion. Determine the saturation point and V_{DSQ} Also calculate the input power, output power and the efficiency.	10	2	L3