

Reg. No.:

Name :



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of U.G. Act 1956)

Continuous Assessment Test I – May 2023

Programme	: B.Tech (ECM)	Semester	: Fall Inter 2022-23
Course	: Computer Architecture and Organization	Code	: BCSE205L
Faculty	: Dr. Sindhuja M Dr. Sunil Kumar Pradhan Dr. Balakrishnan R Mr. Ajeyprasaath Kb	Slot	: A2+TA2
Time	: 90 Minutes	Class Nbr.	: CH2022232500336 CH2022232500337 CH2022232500338 CH2022232500340
		Max. Marks	: 50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks															
		(a) Explain the internal structure of an IAS computer using a neat diagram.	5															
		(b) Suppose for an implementation of a RISC ISA there are 4 instruction types, with their frequency of occurrence and CPI as shown	5															
1.		<table border="1"><thead><tr><th>Type</th><th>Frequency</th><th>CPI</th></tr></thead><tbody><tr><td>LOAD</td><td>20%</td><td>4</td></tr><tr><td>STORE</td><td>8%</td><td>3</td></tr><tr><td>ALU</td><td>60%</td><td>1</td></tr><tr><td>BRANCH</td><td>12%</td><td>2</td></tr></tbody></table> <p>Calculate average CPI.</p>	Type	Frequency	CPI	LOAD	20%	4	STORE	8%	3	ALU	60%	1	BRANCH	12%	2	
Type	Frequency	CPI																
LOAD	20%	4																
STORE	8%	3																
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2.		(a) Tabulate the difference between RISC and CISC Architectures.	5															
		(b) Draw the block diagram of the Harvard architecture and explain why is Harvard architecture faster than Von Neumann?	5															

- (a) Draw the flow chart of booth's algorithm.
- (b) Show the steps of multiplication performed by using booth's algorithm of $(-12) \times (4)$
3. (c) Draw the flow chart of restoring division algorithm 10
- (d) Divide the following binary format positive numbers using the restoring division algorithm: $A = 10101$, $B = 00011$, and verify your answer by converting A and B and your result (A / B) to decimal.
4. What are the advantages of hardwired control unit? Describe the design of hardwired control unit of CPU, with diagram. 10
- Let's consider three different processors P1, P2 and P3 and they execute the same instruction set. P1 processor has 3GHz clock rate and a CPI (Cycles Per Instructions) of 1.5, P2 processor has a clock rate of 2.5 GHz and a CPI of 1.0 and P3 processor has 4.0 GHz clock rate and has a CPI of 2.2.
- (a) Which processor has the highest performance expressed in instructions per second?
5. (b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions? 10
- (c) Let's consider a situation, where the execution time is reduced by 30%, which result an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

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