VIT
Vellore Institute of Technology

Reg. No

Final Assessment Test (FAT) - July/August 2023

Programme	B.Tech.	Semester	Fall Inter Semester 22-23
Course Title	COMPUTER ARCHITECTURE AND ORGANIZATION	Course Code	BCSE205L
Faculty Name	Prof. Sindhuja M	Slot	A2+TA2
		Class Nbr	CH2022232500336
Time	3 Hours	Max. Marks	100

Part A (10 X 10 Marks)
Answer All questions

01. (a) Explain and illustrate any 3 bus structures available. **[10]**
(b) Compare and differentiate between Von Neumann and Harvard Architecture.

02. Explain 5-bit booth multiplier using the flowchart and find the result to multiply (–9) × (–13). **[10]**

03. Divide 11 (eleven) by 3 (three) using non-restoring method and explain the steps involved. **[10]**

04. (a)Consider a MIPS computer with a processor speed of 1GHZ and each ALU instruction takes 3 clock cycles, branch/jump instruction takes 2 clock cycles, each short word (SW) instruction takes 4 clock cycles and each long word(LW) instruction takes 5 clock cycles. Consider a bench mark program which takes 200 million ALU instructions, 55 million branching instructions, 25 million SW instructions and 20 million LW instructions. Find (i) CPI and (ii) CPU time. **[10]**
(b) A two-byte relative mode branch instruction is stored in memory location 1000. The branch is made to the location 87. What is the effective address?

05. (a)Consider a system in which bus cycles takes 500 ns. Transfer of bus control in either direction, from processor to I/O device or vice versa, takes 250 ns. One of the I/O devices has a data transfer rate of 50 KB/s and employs DMA. Data are transferred 1 byte at a time. Suppose we employ DMA in a burst mode. That is, the DMA interface gains bus mastership prior to the start of a block transfer and maintains control of the bus until the whole block is transferred. For how long would the device tie up the bus when transferring a block of 128 bytes? Repeat the calculation for cycle-stealing mode. **[10]**
(b)Explain the interrupt priority system using polling method.

06. (a)A two-way set associative cache memory uses block of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128K X 32.Formulate all pertained information required to construct the cache memory (Tag, Index, Data, blocks, words). **[10]**
(b) What is the size of the cache memory?

07. The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80% of the memory requests are for read and the remaining 20% is for write. The hit ratio for read access is 0.9. A write through procedure is used. **[10]**
(a)What is the average access time of the system considering only memory read cycle?
(b)What is the average access time of the system for both read and write cycles?
(c)What is the hit ratio taking into consideration the write cycles?

08. (a) A bit stream 10011101 is transmitted using the standard CRC method. The generator polynomial is x^3+1. What is the actual bit string transmitted? Suppose the third bit from the left is inverted during transmission. How will receiver detect this error ? [10]

(b) Explain the organization of magnetic disk with Read / Write Mechanism.

09. (a) What is Flynn's classification of computer architecture ? and explain each classification with block diagram. [10]

(b) Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate

i) Pipeline cycle time

ii) Pipeline time for 1000 tasks

iii) Sequential time for 1000 tasks

10. (a) Explain the difference between superscalar and super pipeline architecture with block diagram. [10]

(b) Consider a non-pipelined processor with a clock speed of 2.5 MHz and average cycles per instruction of 4. The same processor is upgraded to a five stage pipelined RISC processor but due to the internal pipeline delay, the clock speed is reduced to 2 MHz Assume there are no stalls in the pipeline. Calculate

i) Cycle Time in Non-Pipelined Processor

ii) Non-Pipeline Execution Time

iii) Cycle Time in Pipelined Processor

iv) Pipeline Execution Time

v) Speed Up ratio

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