VIT

Vellore Institute of Technology

Final Assessment Test – November/December 2023

Course: **CSI1004 - Computer Organization and Architecture**

Class NBR(s): **4085/4087/4090** Slot: **F1+TF1**

Time: **Three Hours** Max. Marks: **100**

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Summarize the actions taken by the IAS processor to carry out the following program instructions. Suppose that program is stored in main memory.

MEMORY

800. LOAD M(X) 1000, DIV M(X) 1001

801. STOR M(X) 1001, (OTHER INST.)

Where 800, 801, 1000, 1001 and 1002 are the addresses for the instructions and data.

2. Solve the following arithmetic statement and write the program:

Y=(A+B*((C/D)*(E-G)))

i) Using an accumulator type computer.

ii) Using a Stack based computer.

iii) Using a general register computer with two address instructions.

iv) Using a general register computer with three address instructions.

3. a) Let us consider the assembly language program given below. **[5]**

The program consists of 5 instructions.

Register R1 content is 3000

Content of 2000 is 1000

Content of 1000 is 500

Content of 2999 is 500

(Note: Each instruction depends on each other)

	Content
LOAD 2000	1000
ADD @2000	1500+1000=1500
MUL #2	3000
SUB -(R1)	0
STORE R1	0

For the above program instruction, find the type of the addressing mode used, effective address and Content of the registers after the execution.

b) Represent +18.15 floating point numbers in IEEE single precision format and double precision format. **[5]**

4. Construct the hardware architecture and flow chart and display the step-by-step multiplication process of signed magnitude multiplication algorithm when subsequent numbers are multiplied.

Multiplicand = +21

Multiplier = -19

Show the contents of the registers and SC during the multiplication process. Use 5-bit register to accommodate the value.

5. Divide **448** by **-17** by applying a signed magnitude division algorithm and find out the value of the quotient and remainder with the correct sign. Use the 6-bit register to store the values. Show the contents of the flip-flop E and registers A, Q & SC during the process of a division using restoring algorithm with comments.

6. a) A digital computer has a memory unit of 512KB and a cache memory of 2KB words. The cache uses direct mapping with a block size of 8 words. How many bits are there in the tag, block and word fields of the address format? **[5]**

   b) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 32,768 blocks and each block contains 512 eight bit Words. How many bits are required for addressing the main memory? How many bits are needed to represent the TAG, SET and WORD fields? **[5]**

7. Consider the following page reference string:

   7, 6, 4, 2, 3, 4, 5, 3, 2, 6, 7, 3, 2, 3, 4, 8, 7, 4, 3, 2, 3, 4, 7.

   How many page faults would occur for the FIFO and LRU replacement algorithms, assuming four frames? Also calculate Hit ratio and Miss ratio. Remember all frames are initially not empty, so your first unique pages will all cost one fault each.

8. Consider CPU and Input/output devices wants to communicate with each other. Explain how the above specified communication takes place in program controlled and Interrupt Initiated Input Output communication process.

9. Explain in detail about various levels of RAID Architecture.

10. Explain in detail about Flynn's taxonomy of parallel machine models.

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