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SCHOOL OF ELECTRONICS ENGINEERING
Fall Semester 2023-2024
CAT- II

Date: 20.10.23 (FN)
Course: BECE102 - Digital Logic Design **B. Tech (ECE)**
Slot: F2 + TF2 **Max. Marks: 50**
Class Nbr: VL2023240102284, VL2023240102278, VL2023240102280, VL2023240102286, VL2023240102282, VL2023240102276

Answer all the Question

Q. No.	Question	Marks	CO	BL
1.	Design a circuit that compares two binary numbers X and Y, each having two bits ($X = X_2 X_1$; $Y = Y_1 Y_2$). It has two outputs A & C. (i) A is supposed to be 1 when $X > Y$ (ii) C is 1 when $X = Y$. Do not use adders/subtractor for this design; instead use a fundamental design process. Draw the minimum sum-of-products circuit. Assume complemented inputs are NOT available, but multiple input gates can be considered.	10	3	4
2.	Design a Synchronous MOD 11 counter using D- FF. Write the Behavioural level HDL for the Flip-Flop and structural level HDL for counter.	10	2	3
3.	Assume that the exclusive-OR gate has a propagation delay of 12ns and that the AND & OR gates have a propagation delay of 4 ns & 2 ns respectively. (a) What is the propagation delay time of full adder? (b) What is the total propagation delay time of a 4-bit ripple carry adder built using the 1-bit full adder? (c) What is the total propagation delay time of a 4 bit carry lookahead adder? Include the circuit diagrams.	10	3	5
4.	Convert the JK – Flip Flop using D –Flip Flop. Instead of using external basic gates use Multiplexer to design.	10	4	1
5.	Design a circuit to multiply 4 bits of data ($A_3A_2A_1A_0$) and 2 bits of data (B_1B_0), also implement the same using Verilog HDL structural modelling with test bench.	10	2	2

R. Anitha

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