

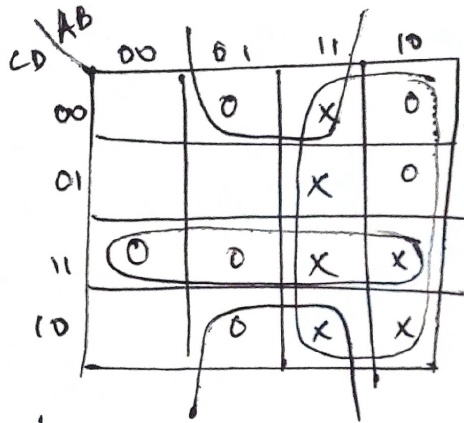
DSD CAT-1 Key

1.a)

$$\begin{aligned}
 y &= \bar{A}C(\overline{ABD}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\
 &= \bar{A}C(A+\bar{B}+\bar{D}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\
 &= \bar{A}A/C + \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\
 &= \bar{B}C(A+\bar{A}) + \bar{A}\bar{D}(C+B\bar{C}) \\
 y &= \bar{B}C + \bar{A}\bar{D}(B+C)
 \end{aligned}$$

(5m)

b) $F(A,B,C,D) = \sum m(0,1,2,5) + d(10,11,12,13,14,15)$



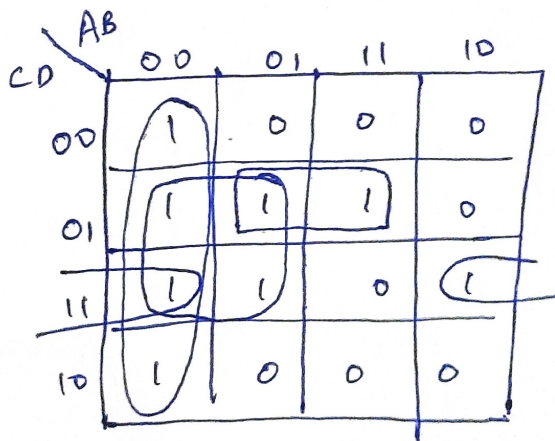
Pos = $\overline{1111}$ (3, 4, 6, 7, 8, 9)

$F(A,B,C,D) = A + CD + B\bar{D}$

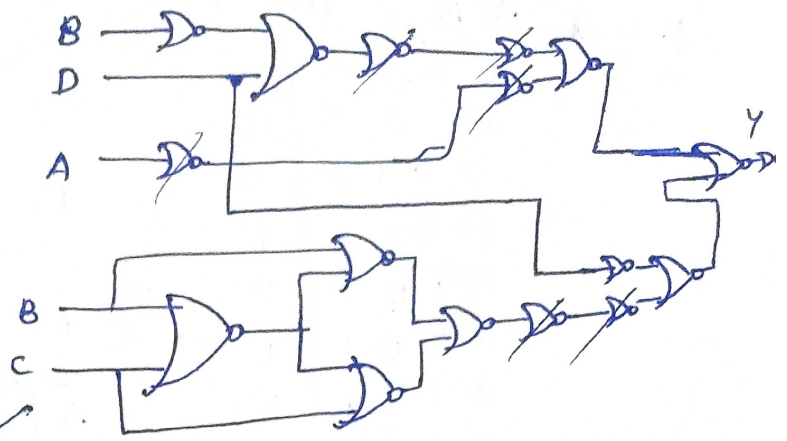
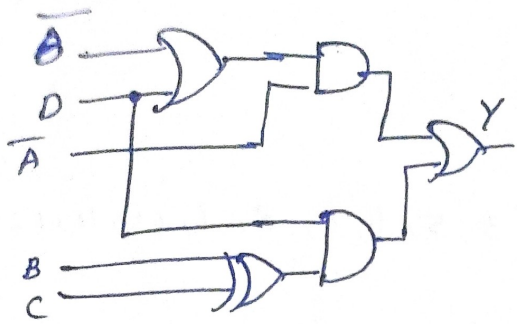
2.

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

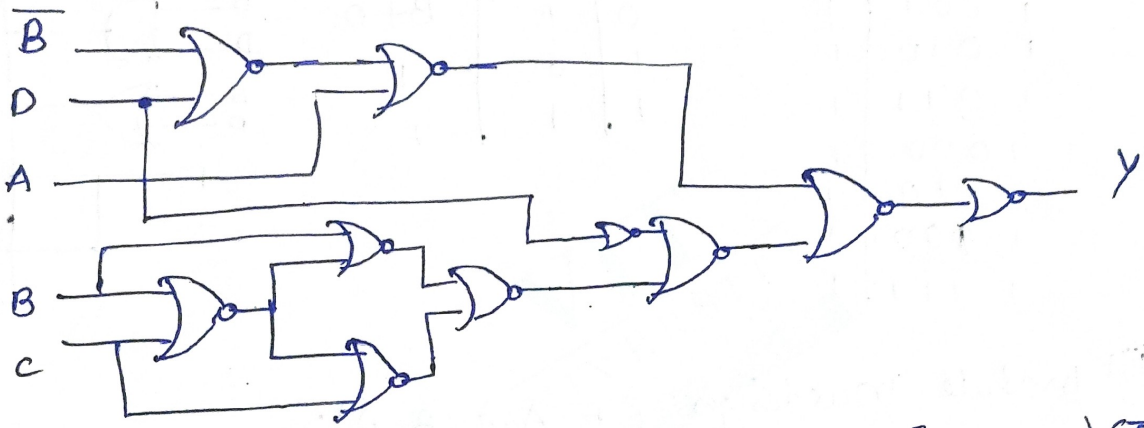
$Y = \sum m(0,1,2,3,5,7,11,13)$



$$\begin{aligned}
 Y &= \bar{A}\bar{B} + \bar{A}D + B\bar{C}D + \bar{B}CD \\
 &= \bar{A}(\bar{B}+D) + D(B\bar{C} + \bar{B}C) \\
 &= \bar{A}(\bar{B}+D) + D(CB \oplus C)
 \end{aligned}$$



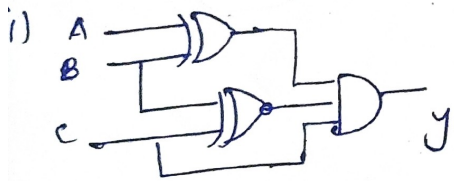
3m



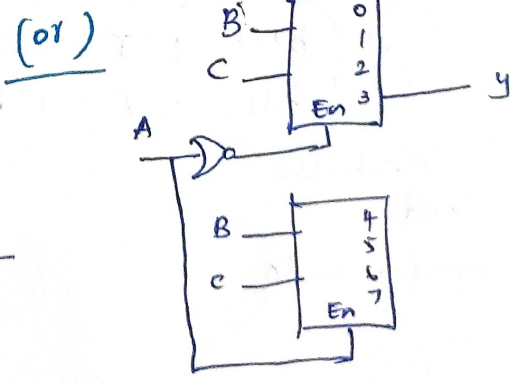
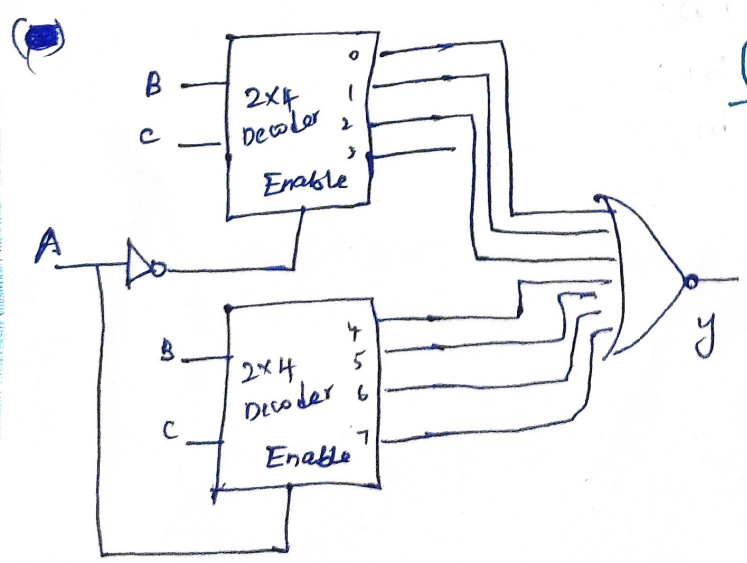
$$y = (A \oplus B) \cdot \overline{(B \oplus C)} \cdot C = (\overline{A}B + A\overline{B}) \cdot (\overline{B}C + BC) \cdot C$$

$$= (\overline{A}B + A\overline{B}) BC$$

$$= \overline{A}BC$$



- (i) $\overline{A}BC$
- (ii) Two decoders



(iv) Minterms connected to nor gate 0,1,2,4,5,6,7

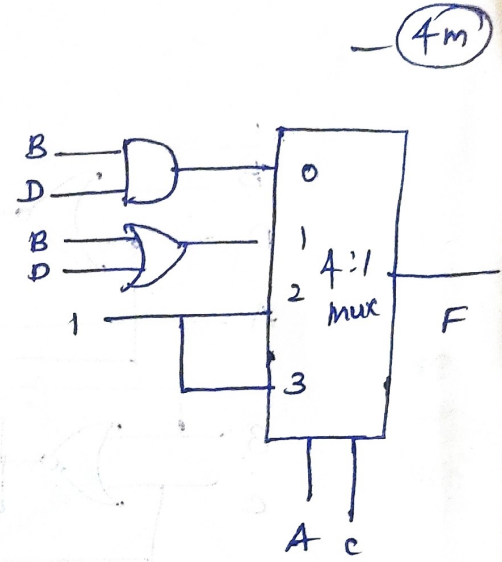
4. (i)

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$F = \sum m(3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)$ — (2m)

(ii) 4:1 Mux with A and C as select lines

Select		Data Input
A	C	
0	0	B D
0	1	B + D
1	0	1
1	1	1



(iii) Module muxdesign (F, A, C, B, D);

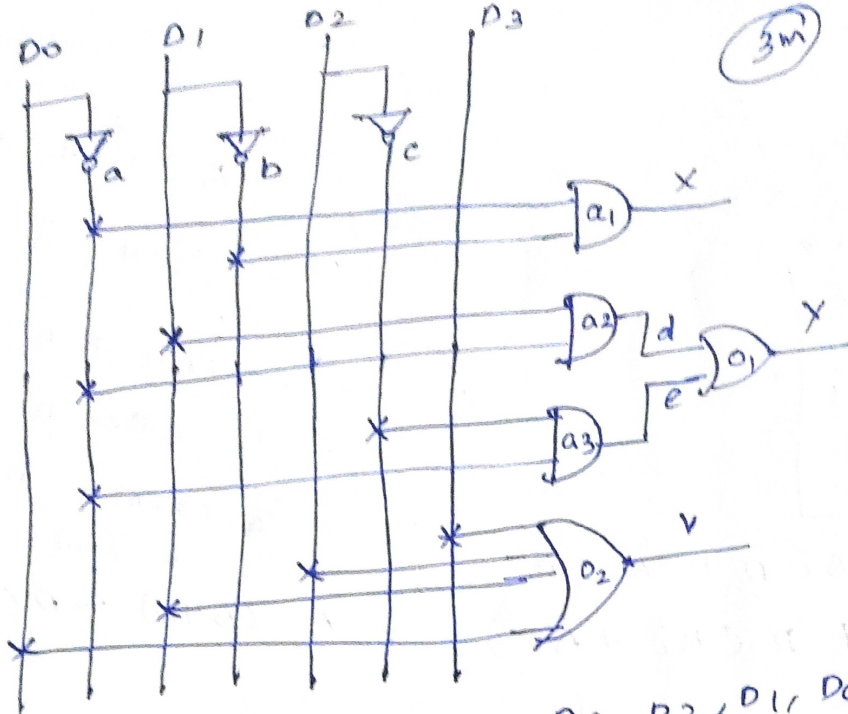
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Input A, C, B, D;
output F;
reg F;
always @ (A, C, B, D)
begin
  case ({A, C})
    2'b00 : F = B & D;
    2'b01 : F = B | D;
    2'b10 : F = 1'b1;
    2'b11 : F = 1'b1;
  endcase
end
endmodule

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— (4m)

5. a)



3M

Module circuit $(X, Y, V, D_3, D_2, D_1, D_0)$;

input D_3, D_2, D_1, D_0 ;

output X, Y, V ;

wire a, b, c, d, e ;

and $a_1 (X, a, b)$;

and $a_2 (d, D_1, a)$;

and $a_3 (e, c, a)$;

or $o_1 (Y, d, e)$;

or $o_2 (V, D_3, D_2, D_1, D_0)$;

endmodule

4M

b)

(i) $\sim x \rightarrow 1$

(ii) $(x > y) ? x : y \rightarrow 1101$

(iii) $\{y, 2\{x[1]\}, z[2]\} \rightarrow 1101110$