Slot: F1+TF1

VIT

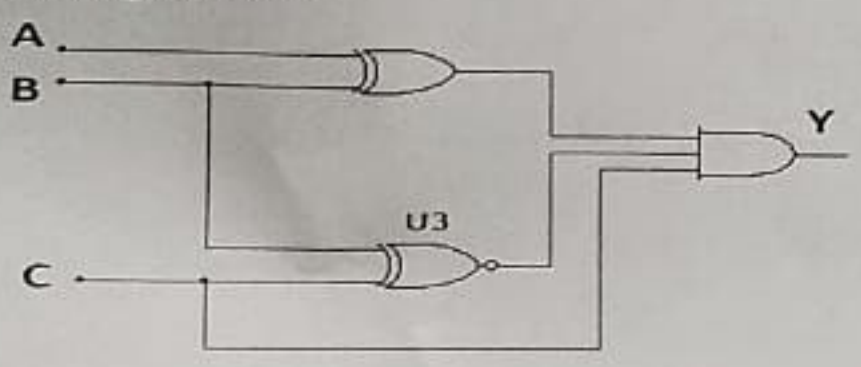
Vellore Institute of Technology

SCHOOL OF ELECTRONICS ENGINEERING
FALL SEMESTER 2023-2024
CAT-I

Programme Name & Branch : B.TECH (ECE, BML)
Course Code & Name : BECE102L Digital Systems Design
Date of the Examination : 15.09.23
Faculty Members: Prof. Sridevi S, Prof.Aarthy M, Prof.Anitha R, Prof.Prayline Rajabai C
Prof. Padmini TN, Prof. Jayakrishnan P
Class Number(s): VL2023240102281, 2279, 2285, 2283, 2275, 2277

Duration: 90 minutes **Max. Marks : 50**

General instruction(s): Answer ALL the questions

No	Question	Marks
1.	a) Simplify the following expression using Boolean Algebra. $Y = \overline{A}\,C\,(\overline{\overline{A}BD}) + \overline{A}\,B\,\overline{C}\,\overline{D} + A\,\overline{B}\,C$ [5Marks] b) Obtain the simplified expression in POS form using K-Map: $F(A,B,C,D) = \sum (0,1,2,5) + d(10,11,12,13,14,15)$ [5Marks]	10
2.	Design a 4 input (A, B, C, D) combinational logic circuit whose output Y is one when the input is a prime number. Consider 0 and 1 as prime numbers. Use K-map to find the simplest possible logic expression in SOP form. Implement the minimal expression using only NOR gates.	10
3.	Analyze the circuit given below.  i. Write the Boolean expression for the given circuit. [2 Marks] ii. Write the output expression in canonical SOP form. [3 Marks] iii. If the circuit has to be implemented using 2x4 Decoders with enable and one NOR gate, how many 2x4 decoders are required. [3 Marks] iv. Each output of the decoder circuit represents a minterm. What minterms should be connected to the input of the NOR gate. [2 Marks]	10

4.	A bank has 4 locks with a key for each lock. Each key is owned by a different person (A, B, C, D). In order to open the vault door at least two people must insert their keys into the assigned locks at the same time. The manager (A) can open the lock alone. The signal lines (A, B, C, D) are 1 if the key is inserted into locks 1,2,3,4 respectively. i. From the truth table, identify the minterms for the digital locking system. [2 Marks] ii. If the circuit is implemented using a 4x1Multiplexer with A and C as the select lines, what will be the data inputs connected to the multiplexer. Write the data inputs connected to the multiplexer in order. [4 Marks] iii. Write the Behavioural Verilog code for part (ii). [4 Marks]	10

5.	a) Write the equivalent Verilog code in gatelevel modelling style, for the given dataflow modelling. In addition give the circuit diagram also. [7 Marks]
	
	module circuit (X,Y,V,D3,D2,D1,D0);
	input D3,D2,D1,D0;
	output X,Y,V
	assign X= (~D1) & (~D0);
	assign Y= (D1 & (~D0)) | ((~D2) & (~D0));
	assign V= D3| D2 | D1| D0;
	endmodule
		10

	b) Find the result of each Verilog expression (in binary) for the following inputs: X = 4'b1010; Y = 4'b1101; Z = 3'b010 i. ~& X [3 Marks] ii. (X > Y) ? X : Y iii. {Y, 2{X[1]}, Z[2]}	