FALL SEMESTER 2023-2024

CAT-2

DIGITAL SYSTEMS DESIGN

1) $F = (X * Y) + Z$

2-bit X $\Rightarrow$ X_1 X_0

2-bit Y $\Rightarrow$ Y_1 Y_0

$X * Y \Rightarrow$ X_1Y_0 X_0Y_0

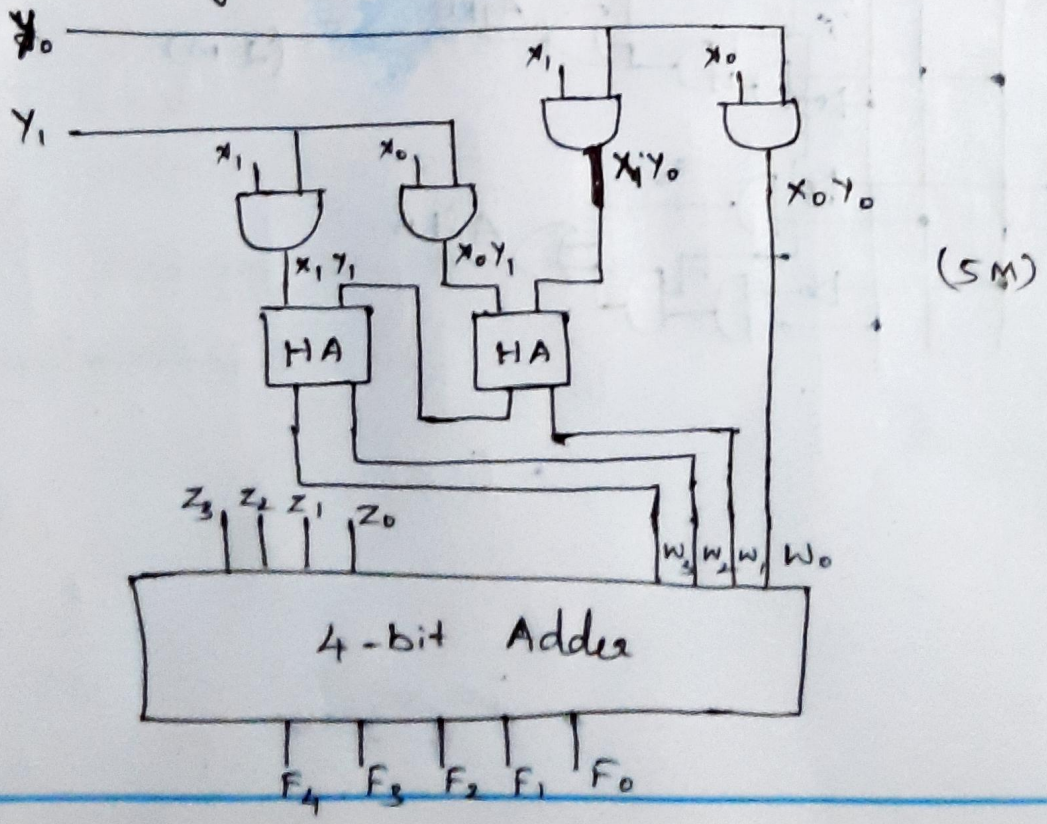
X_1Y_1 X_0Y_1

W_3 W_2 W_1 W_0 (5M)

4-bit Z $\Rightarrow$ Z_3 Z_2 Z_1 Z_0

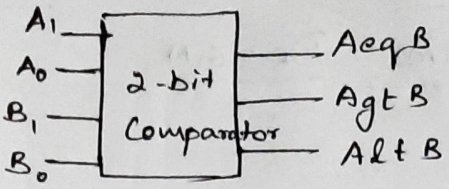
$(X * Y) + Z \Rightarrow F_4$ F_3 F_2 F_1 F_0

Circuit Diagram



(5M)

2 i) 2-bit comparator

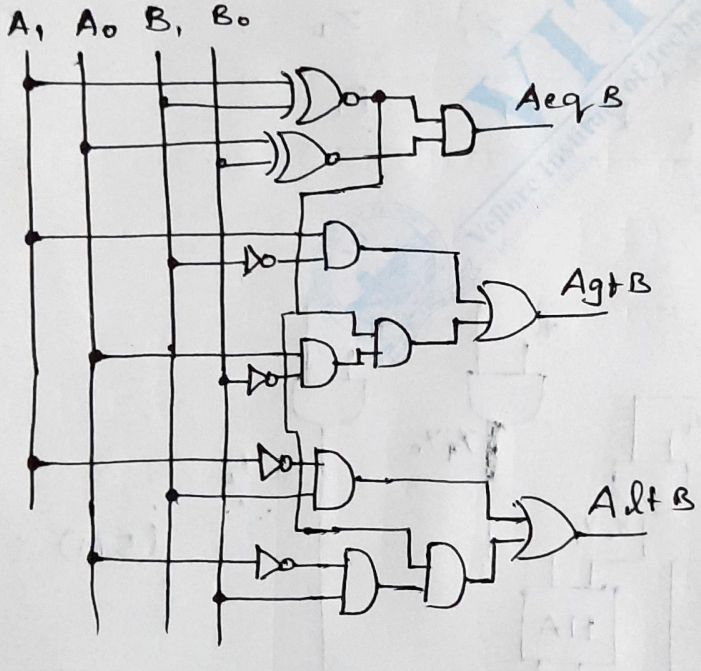


$A_{eq}B = (A_1 \odot B_1) . (A_0 \odot B_0)$

$A_{gt}B = A_1 B_1' + (A_1 \odot B_1) A_0 B_0'$ (3M)

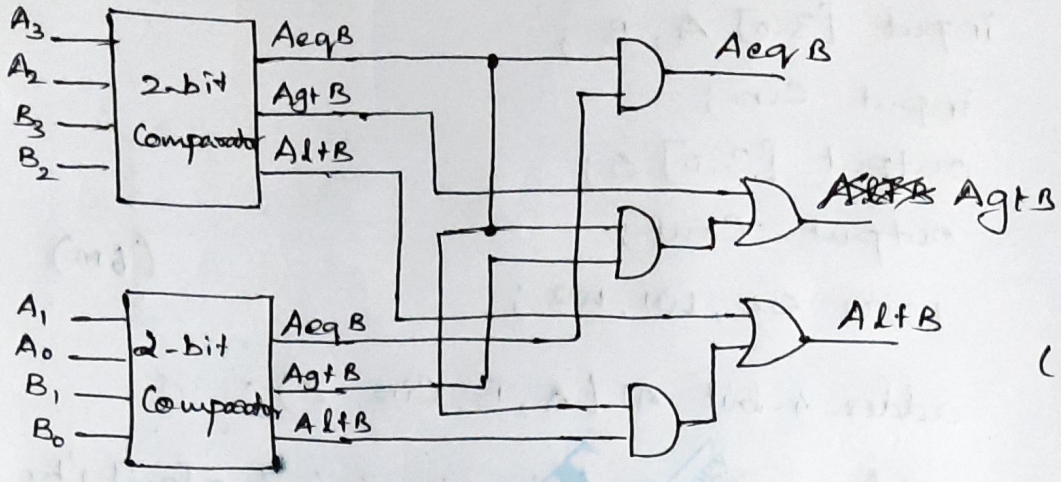
$A_{lt}B = A_1' B_1 + (A_1 \odot B_1) A_0' B_0$

CRT diagram



(2 M)

2 ii) 4-bit Comparator using 2-bit Comparator



(5M)

3) Dataflow Verilog HDL for 4-bit Adder

```
module adder_4-bit (A, B, Cin, Z);
    input [3:0] A, B;
    input Cin;
    output [4:0] Z;
    assign Z = A + B + Cin;
endmodule
```

(4M)

Structural Code for the given Circuit:

```
module ckt (A, B, Cin, S, Cout);
  input [3:0] A, B;
  input Cin;
  output [3:0] S;
  output Cout;
  wire S4, W1, W2;
  adder_4_bit A1 (A, B, Cin, Z);
  adder_4_bit A2 ({3'b0, 2{Cout}, 1'b0}, Z[3:0], 1'b0, {S4, S});
  and G1 (W1, Z[3], Z[2]);
  and G2 (W2, Z[3], Z[1]);
  or G3 (Cout, Z[4], W1, W2);
endmodule
```

(6M)

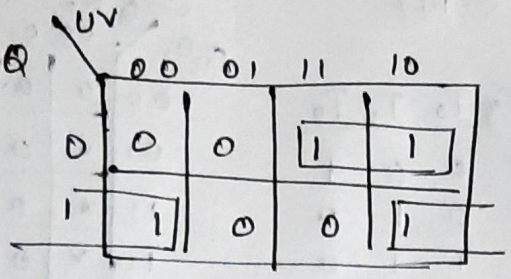
4 i) Excitation table for UV-FF

Q	Q^+	U	V
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(2M)

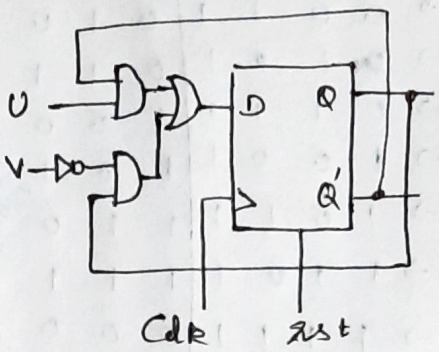
(ii) UV-FF using D-FF

K-map for D-i/p



(4M)

$D = UQ' + V'Q$



For D-FF, $Q^+ = D$

$\therefore Q^+ = UQ' + V'Q$

(iii) Verilog HDL for UV-FF

```
module - UV_FF (clk, rst, U, V, Q);
   input clk, rst, U, V;
   output Q;
   reg Q;
   always @ (posedge clk)
      if (rst)
         Q <= 1'b0;
      else
         case ({U, V})
            2'b00 : Q <= Q;
            2'b01 : Q <= 1'b0;
            2'b10 : Q <= 1'b1;
            2'b11 : Q <= ~Q;
         endcase
endmodule
```

(4M)

5) Synchronous Counter using T-FF for the sequence

↱ 0 → 1 → 3 → 5 → 7 → 9 → 11 → 13 → 15 ↲

State transition table (3M)

	Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	T_3	T_2	T_1	T_0
0 →	0	0	0	0	0	0	0	1	0	0	0	1
1 →	0	0	0	1	0	0	1	1	0	0	1	0
3 →	0	0	1	1	0	1	0	1	0	1	1	0
5 →	0	1	0	1	0	1	1	1	0	0	1	0
7 →	0	1	1	1	1	0	0	1	1	1	1	0
9 →	1	0	0	1	1	0	1	1	0	0	1	0
11 →	1	0	1	1	1	1	0	1	0	1	1	0
13 →	1	1	0	1	1	1	1	1	0	0	1	0
15 →	1	1	1	1	0	0	0	0	1	1	1	1

K-map (4M)

T_3 (rows Q_3Q_2, columns Q_1Q_0):

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	x
01	x	0	1	x
11	x	0	1	x
10	x	0	0	x

$T_3 = Q_2 Q_1$

T_2 (rows Q_3Q_2, columns Q_1Q_0):

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	1	x
01	x	0	1	x
11	x	0	1	x
10	x	0	1	x

$T_2 = Q_1$

T_1 (rows Q_3Q_2, columns Q_1Q_0):

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	1	x
01	x	1	1	x
11	x	1	1	x
10	x	1	1	x

$T_1 = Q_0$

T_0 (rows Q_3Q_2, columns Q_1Q_0):

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	x
01	x	0	0	x
11	x	0	1	x
10	x	0	0	x

$T_0 = Q_0' + Q_3 Q_2 Q_1$

Circuit Diagram : (3M)