

**School of Computer Science Engineering and Information Systems**  
**Fall Semester 2023-2024**

**Open Book Exam-Continuous Assessment Test – II: KEY**

**Programme Name & Branch:** BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

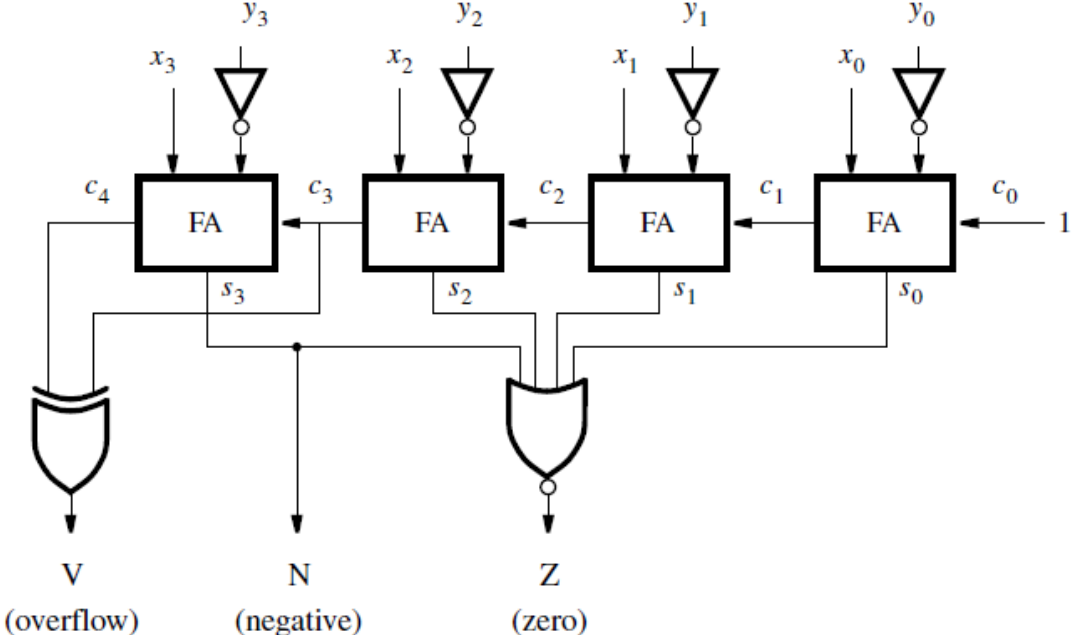
**Course Name & code:** BECE102L & Digital Systems Design

**Slot:** B1+TB1

**Exam Duration:** 90 Min.

**Maximum Marks:** 50

*Answer all the questions*

Q. No.	Question	Max Marks
1.	<p>One arithmetic circuit is shown in Figure 1; it contains four 1-bit Full Adder (FA). Write the Verilog code using structural modeling to specify the operation of the arithmetic circuit and also write its test bench.</p> <p><b>Note:</b> The individual FA should be designed by Data flow modeling.</p> <div style="text-align: center;">  <p style="text-align: center;">Figure.1</p> </div>	10

## Solution :

```
module comparator (X, Y, V, N, Z);
  input [3:0] X, Y;
  output V, N, Z;
  wire [3:0] S;
  wire [4:1] C;

  fulladd stage0 (1'b1, X[0], ~Y[0], S[0], C[1]);
  fulladd stage1 (C[1], X[1], ~Y[1], S[1], C[2]);
  fulladd stage2 (C[2], X[2], ~Y[2], S[2], C[3]);
  fulladd stage3 (C[3], X[3], ~Y[3], S[3], C[4]);
  assign V = C[4] ^ C[3];
  assign N = S[3];
  assign Z = !S;

endmodule

module fulladd (Cin, x, y, s, Cout);
  input Cin, x, y;
  output s, Cout;

  assign s = x ^ y ^ Cin;
  assign Cout = (x & y) | (x & Cin) | (y & Cin);

endmodule
```

## Test Bench :

```
module tb_comparator;
  reg [3:0] X, Y;
  wire V, N, Z;
  // Instantiate the comparator module
  comparator u1 (.X(X), .Y(Y), .V(V), .N(N), .Z(Z));

  initial begin
    X = 4'b1010; // You can change these values
    Y = 4'b1101; // to test different cases
    // Apply different test case

    // Test case 1
    #10 X = 4'b0011;
    #10 Y = 4'b1100;

    // Test case 2
    #10 X = 4'b1010;
    #10 Y = 4'b0101;

    // Test case 3
    #10 X = 4'b1111;
    #10 Y = 4'b0000;
  end

endmodule
```

Assume that registers M and Q of the sequential Booth's multiplier are initialized with the values -15 and 10.

- i. Perform the multiplication operation according to Booth's algorithm.
- ii. After multiplication, how many subtraction and addition operations will be performed? Write the answer in decimal.
- iii. Write the logical block diagram that implements the Booth's multiplier.

**Note:** Consider M (6 bit) = Multiplicand and Q (6Bit) = Multiplier

**Solution : (i)**

Handwritten solution for Booth's multiplication:

$(-15) \times (10)$   
 $M \times Q$   
 $M : (110001)_2$   
 $-M : (001111)_2$   
 $Q : (001010)_2$   
 Product = -150

Multiplication:  
 $150 \Rightarrow (000010010110)_2$   
 $\downarrow$  1's complement  
 $111101101001$   
 $+ 1$   
 $-150 \Rightarrow 111101101010$

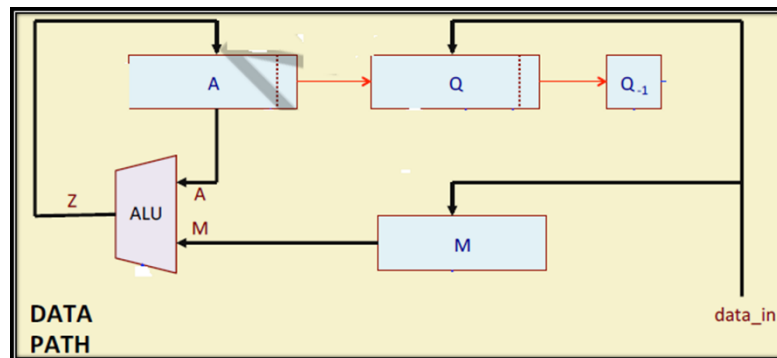
A	Q	Q <sub>-1</sub>	Operation
0 0 0 0 0 0	0 0 1 0 1 0	0	initial ✓
0 0 0 0 0 0	0 0 0 1 0 1	0	shift
0 0 1 1 1 1	0 0 0 1 0 1	0	A = A - M
0 0 0 1 1 1	1 0 0 0 1 0	1	shift
1 1 1 0 0 0	1 0 0 0 1 0	1	A = A + M
1 1 1 1 0 0	0 1 0 0 0 1	0	shift
0 0 1 0 1 1	0 1 0 0 0 1	0	A = A - M
0 0 0 1 0 1	1 0 1 0 0 0	0	shift
1 1 0 1 1 0	1 0 1 0 0 0	0	A = A + M
1 1 1 0 1 1	0 1 0 1 0 0	0	shift
1 1 1 1 0 1	1 0 1 0 1 0	0	

2.

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(ii) 2 Subtraction and 2 Addition

(iii)



A New clocked A-B Flip-Flop is defined with two inputs, A and B, in addition to the clocked input. Refer the table for the flip flop function.

CLK	A	B	$Q_{n+1}$
0	x	x	$Q_n$
↑	0	0	1
↑	0	1	$Q_n$
↑	1	0	$Q_n$
↑	1	1	0

- Provide the Characteristics table and Characteristic equation for the A-B flip flop.
- Provide the Excitation table and input equations.
- Implement the A-B flip flop using a D flip flop.

**Solution :**

**Part (i) :**

3.

① characteristic table:

$Q_n$	A	B	$Q_{n+1}$
0	0	0	1
1	0	0	0
2	0	1	0
3	0	1	0
4	1	0	1
5	1	0	1
6	1	1	0
7	1	1	0

② char. equation.

for  $Q_{n+1} =$

Karnaugh Map:

$Q_n$	AB	$\bar{A}B$	$A\bar{B}$	$\bar{A}\bar{B}$
$\bar{Q}_n$	1	0	0	0
$Q_n$	1	1	0	0

Groupings: I (minterms 4, 5), II (minterms 0, 1), III (minterms 2, 3), IV (minterm 6).

Characteristic Equation:

$$Q_{n+1} = I + II + III$$

$$= Q_n \bar{A} + \bar{A} \bar{B} + Q_n \bar{B}$$

$$= Q_n (\bar{A} + \bar{B}) + \bar{A} \bar{B}$$

$Q_{n+1} = \sum m(0, 4, 5, 6)$

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**Part (ii) :**

Excitation table

$\phi_n$	$\phi_{n+1}$	A	B
0	0	0	0
0	1	0	0
1	0	1	1
1	1	0	0

for A

$\phi_n$	$\phi_{n+1}$	$\phi_{n+1}$
$\bar{\phi}_n$	X	0
$\phi_n$	1	X

$A = \phi_n$   
 $A = \phi_{n+1}$

for B

$\phi_n$	$\phi_{n+1}$	$\phi_{n+1}$
$\bar{\phi}_n$	X	0
$\phi_n$	1	X

$B = \phi_n$   
 $B = \phi_{n+1}$

**Part (iii) :**

D to A-B conversion

step-1  
 AV FF = D FF  
 req FF = A-B FF

step-2 make ch. table for req FF

$\phi_n$	A	B	$\phi_{n+1}$	D
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

for D

$\phi_n$	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$AB$
$\bar{\phi}_n$	1			
$\phi_n$		1	1	

$D = I + II + III$   
 $= \bar{\phi}_n \bar{A} + \bar{A} \bar{B} + \phi_n \bar{B}$   
 $D = \phi_n (\bar{A} + \bar{B}) + \bar{A} \bar{B}$

step-3 make excitation table for AV FF

$\phi_n$	$\phi_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

step-4 final ch

A 4-bit shift register circuit is configured for right-shift operation is  $D_{in}$  to  $Q_1$ ,  $Q_1$  to  $Q_2$ ,  $Q_2$  to  $Q_3$ ,  $Q_3$  to  $Q_4$ , is shown in Figure. 2. If the present state of the shift register is  $Q_1Q_2Q_3Q_4=0110$

- i. Write the truth table and timing diagram for 8 number of clock cycle .
- ii. Calculate the number of clock cycles required to reach the state  $Q_1Q_2Q_3Q_4=1111$
- iii. Implement Verilog model of the given diagram

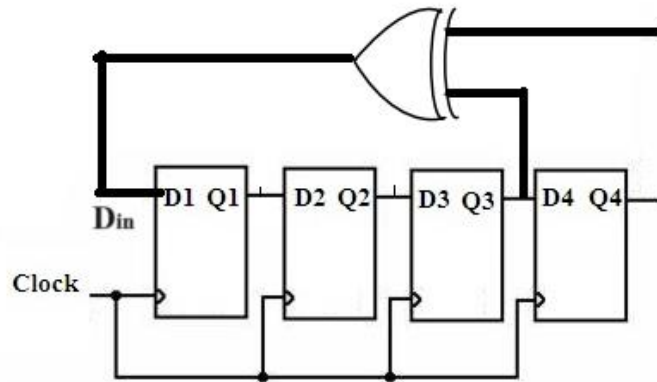


Figure.2

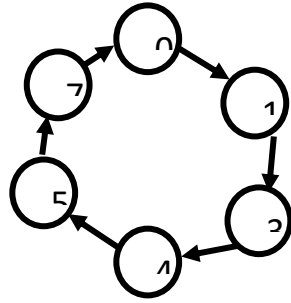
4.

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**Solution :**

Clock	Q1	Q2	Q3	Q4	Din = Q3 exor Q4
0	0	1	1	0	1
1	1	0	1	1	0
2	0	1	0	1	1
3	1	0	1	0	1
4	1	1	0	1	1
5	1	1	1	0	1
<b>6</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>0</b>
7	0	1	1	1	0
8	0	0	1	1	0

Design a counter for the given sequence as shown in the Figure.3 using T Flip flop.



**Solution :** State transition table for given sequence:

Present State			Next State			Input table of Flip-Flops		
Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>3</sub> (t+1)	Q <sub>2</sub> (t+1)	Q <sub>1</sub> (t+1)	T <sub>3</sub>	T <sub>2</sub>	T <sub>1</sub>
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	0	1	0
1	1	1	0	0	0	1	1	1

5.

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Solve the above table For T<sub>3</sub>, T<sub>2</sub> and T<sub>1</sub> using 3 variable k Map and consider 2 and 6 position as don't care (×)

$$T_3 = Q_2$$

$$T_2 = Q_1$$

$$T_1 = Q_2 + Q_1'$$

