

School of Computer Science Engineering and Information Systems

Fall Semester 2023-2024

Continuous Assessment Test – II

Programme Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE102L Digital Systems Design

Slot:

B2+TB2

Exam Duration: 90 Min.

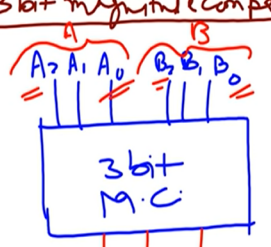
Maximum Marks: 50

General instruction(s): Answer all the questions

Q. No	Question	Max Marks
1.	<p>Obtain the Boolean expressions ($A > B$, $A = B$ and $A < B$) for 3-bit magnitude comparator. Based on the comparison, develop a control network to perform the following operation in block diagram level.</p> <ol style="list-style-type: none"> If $A = B$, Perform array multiplication If $A > B$, Perform two complement subtraction If $A < B$, Perform binary addition. 	10

kishore's Notebook > Digital Circuits

3 bit magnitude comparator:



$A = B, A_2 = B_2, A_1 = B_1, A_0 = B_0$

$A_2 = B_2, \chi_2 = \bar{A}_2 B_2 + A_2 \bar{B}_2$

$A_1 = B_1, \chi_1 = \bar{A}_1 B_1 + A_1 \bar{B}_1$

$A_0 = B_0, \chi_0 = \bar{A}_0 B_0 + A_0 \bar{B}_0$

$E = \chi_2 \cdot \chi_1 \cdot \chi_0$

$A < B, \text{ IF } \underline{A_2 < B_2}$

OR

$\text{IF } A_2 = B_2, \underline{A_1 < B_1}$

OR

$\text{IF } A_2 = B_2 \text{ and } A_1 = B_1, \underline{A_0 < B_0}$

$L = \bar{A}_2 B_2 + \chi_2 \cdot A_1 B_1 + \chi_2 \chi_1 \cdot \bar{A}_0 B_0$

$A > B, \text{ IF } \underline{A_2 > B_2}$

OR

$\text{IF } A_2 = B_2, \text{ then } \underline{A_1 > B_1}$

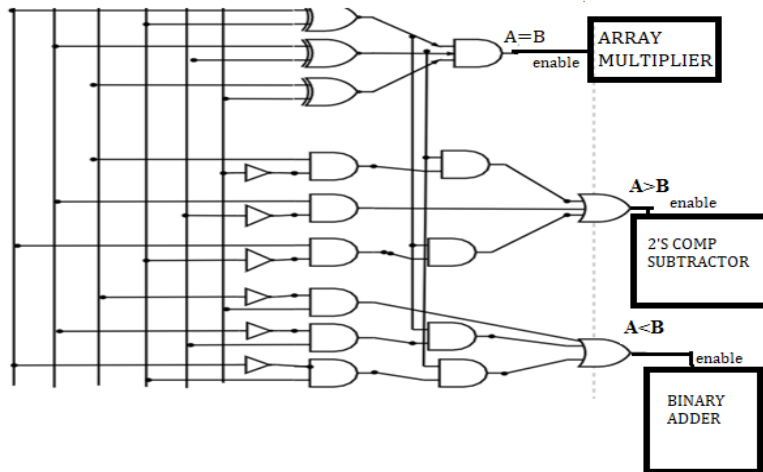
OR

$\text{IF } A_2 = B_2, A_1 = B_1, \text{ then } \underline{A_0 > B_0}$

$G = A_2 \bar{B}_2 + \chi_2 \cdot A_1 \bar{B}_1 + \chi_2 \chi_1 \cdot A_0 \bar{B}_0$

LOGIC GATE STUDIES

$$A < B = A_2'B_2 + [(A_2'B_2' + A_2B_2) * A_1'B_1] + [(A_2'B_2' + A_2B_2) * [(A_1'B_1' + A_1B_1) * A_0'B_0]]$$

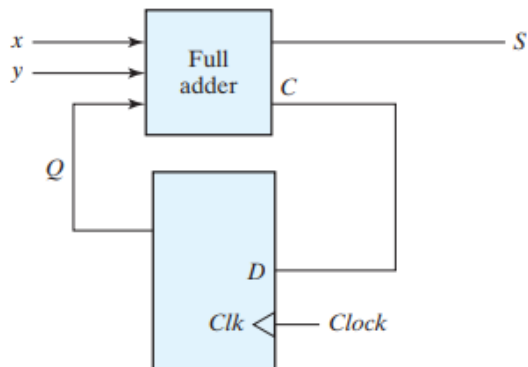


$$A < B = A_2'B_2 + [(A_2'B_2' + A_2B_2) * A_1'B_1] + [(A_2'B_2' + A_2B_2) * [(A_1'B_1' + A_1B_1) * A_0'B_0]]$$

Internal circuits for all the three blocks is required

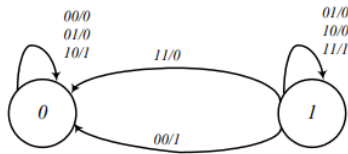
2. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Figure 3. Derive the state table and state diagram of the sequential circuit.

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Solution:

Present state	Inputs		Next state	Output
	Q	S		
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$S = x \oplus y \oplus Q$$

$$Q(t+1) = xy + xQ + yQ$$

3. A new clocked X-Y flip-flop is defined with two inputs, X and Y in addition to the clocked input. The flip flop functions as follows:
- If XY=01, the flip flop state (Q) becomes 1 at the next clock pulse
 - If XY=10, the flip flop state (Q) becomes 0 at the next clock pulse.
 - If X=Y, the flip flop toggles its state (Q) at the next clock pulse.
- i. Provide the truth table for the X-Y flip flop
 - ii. Provide the characteristics table
 - iii. Provide the Excitation table for the X-Y flip flop
 - iv. Implement X-Y flip flop using a J-K flip flop
 - v. Write the Verilog code for final implemented circuit using behavioral modeling.

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① Truth-table

X	Y	Q ⁺
0	0	0
0	1	1
1	0	0
1	1	Q̄

② Ch. Table

Q	X	Y	Q ⁺
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

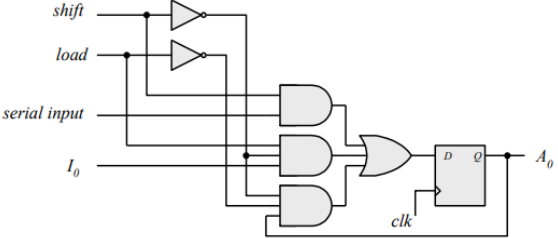
③ Excitation-table

Q	Q ⁺	X	Y
0	0	1	0
0	1	0	1
1	0	1	0
1	1	1	1

④ J-K to X-Y. Excitation-table of J-K FF.

Q	Q ⁺	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$J = \sum m(0, 1, 3) + d(4, 5, 6, 7)$
 $K = \sum m(4, 6, 7) + d(0, 1, 2, 3)$
 $J = X + Y$
 $K = X + Y$

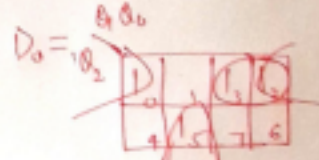
4.	<p>Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change.</p> <p>Solution:</p> <p>First stage of register:</p> 	10
5.	<p>Design a synchronous counter for the count sequence 0-3-5-7-2-1-0 using positive edge triggered D flip-flop. Write the Verilog code for the designed flip flop.</p>	10

Solution:-
Count sequence $\rightarrow 0-3-5-7-2-1-0$

no. of ff = 3



B_2	B_1	B_0	PS	B_2^+	B_1^+	B_0^+	D_2	D_1	D_0
0	0	0	0	0	1	1	0	1	1
0	1	1	1	0	1	1	1	0	1
1	0	1	1	1	1	1	1	1	1
1	1	1	0	1	0	0	0	1	0
0	1	0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0	0



$$D_0 = \bar{B}_2 B_0 + \bar{B}_2 \bar{B}_0$$

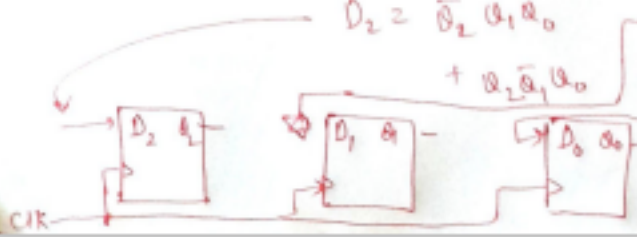


$$D_1 = \bar{B}_2 \bar{B}_1 \bar{B}_0 + \bar{B}_2 B_1 \bar{B}_0$$



$$D_2 = \bar{B}_2 B_1 B_0 + B_2 \bar{B}_1 B_0$$

$$D_0 = \bar{B}_2 (B_1 + \bar{B}_0)$$



NOTE*: Please refer below to the BL – Bloom's Taxonomy Levels and mention the respective

level in the questions.

Bloom's Taxonomy Levels	Category
BL1	Remembering
BL2	Understanding
BL3	Applying
BL4	Analyzing
BL5	Evaluating
BL6	Creating