VIT
Vellore Institute of Technology

School of Computer Science Engineering and Information Systems

Fall Semester 2023-2024

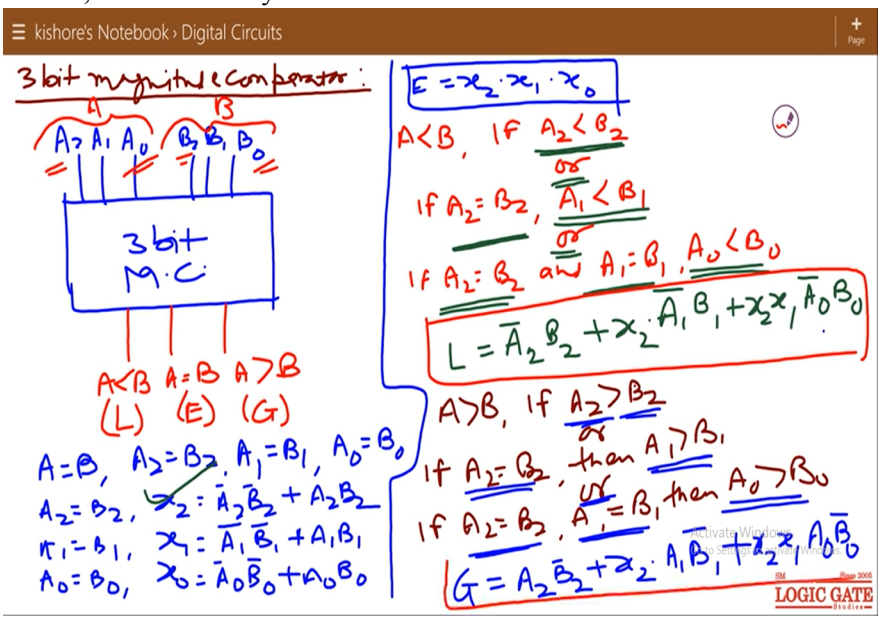
Continuous Assessment Test – II

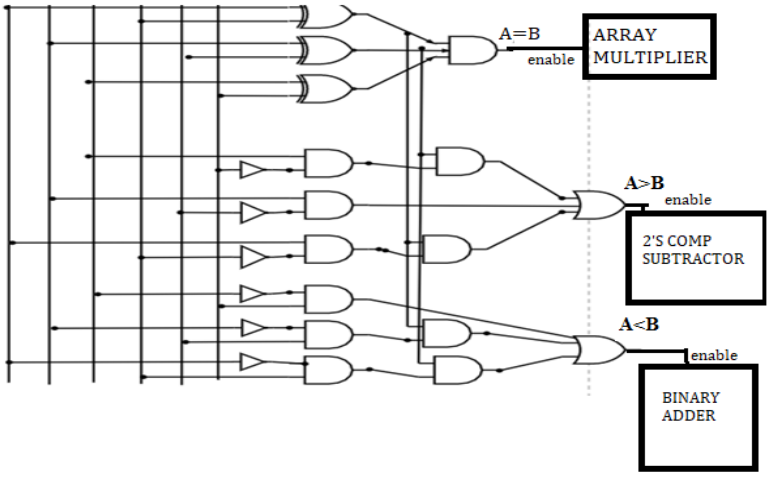
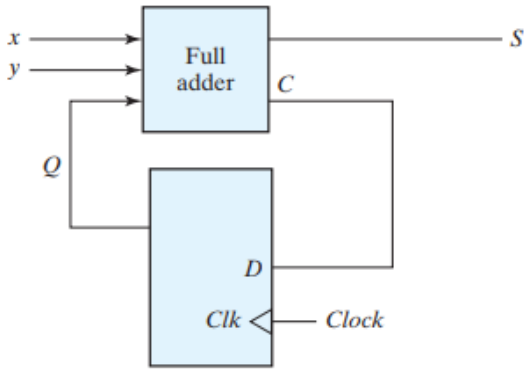
Programme Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE102L Digital Systems Design **Slot:** **B2+TB2**

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s): *Answer all the questions*

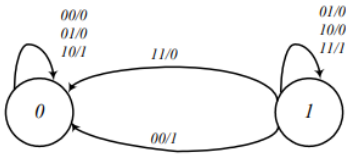
Q. No.	Question	Max Marks
1.	Obtain the Boolean expressions (A>B, A=B and A<B) for 3-bit magnitude comparator. Based on the comparison, develop a control network to perform the following operation in block diagram level. a. If A=B, Perform array multiplication b. If A>B, Perform two complement subtraction c. If A<B, Perform binary addition. 	**10**

	A<B = A2'B2 + [(A2'B2' + A2B2) * A1'B1] + [(A2'B2' + A2B2) *[(A1'B' + A1B1) * A0'B0]  A<B = A2'B2 + [(A2'B2' + A2B2) * A1'B1] + [(A2'B2' + A2B2) *[(A1'B' + A1B1) * A0'B0] ***Internal circuits for all the three blocks is required***	
2.	A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Figure 3. Derive the state table and state diagram of the sequential circuit.  Solution:	**10**

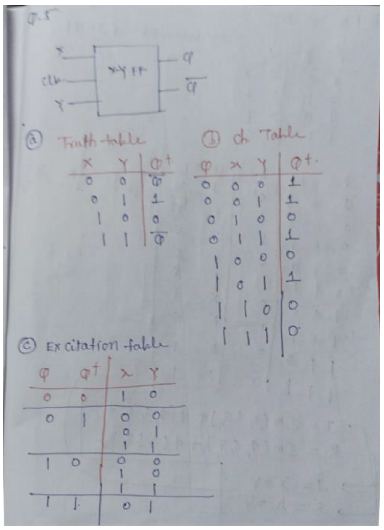
Present state	Inputs		Next state	Output
Q	x	y	Q	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

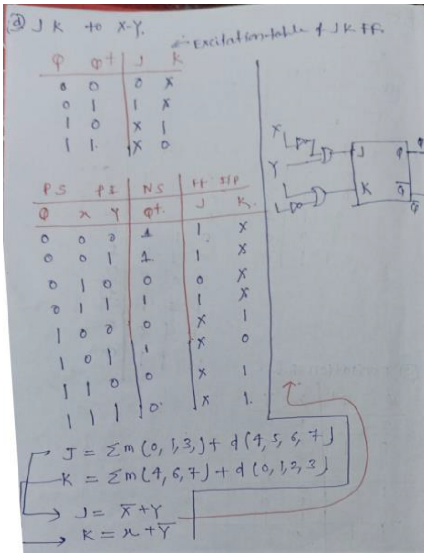
$S = x \oplus y \oplus Q$

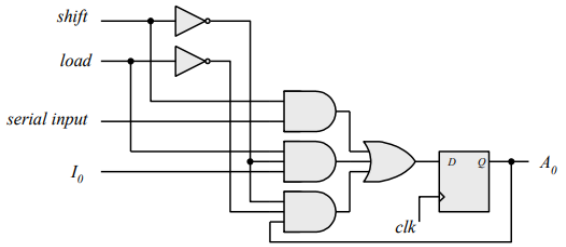
$Q(t+1) = xy + xQ + yQ$

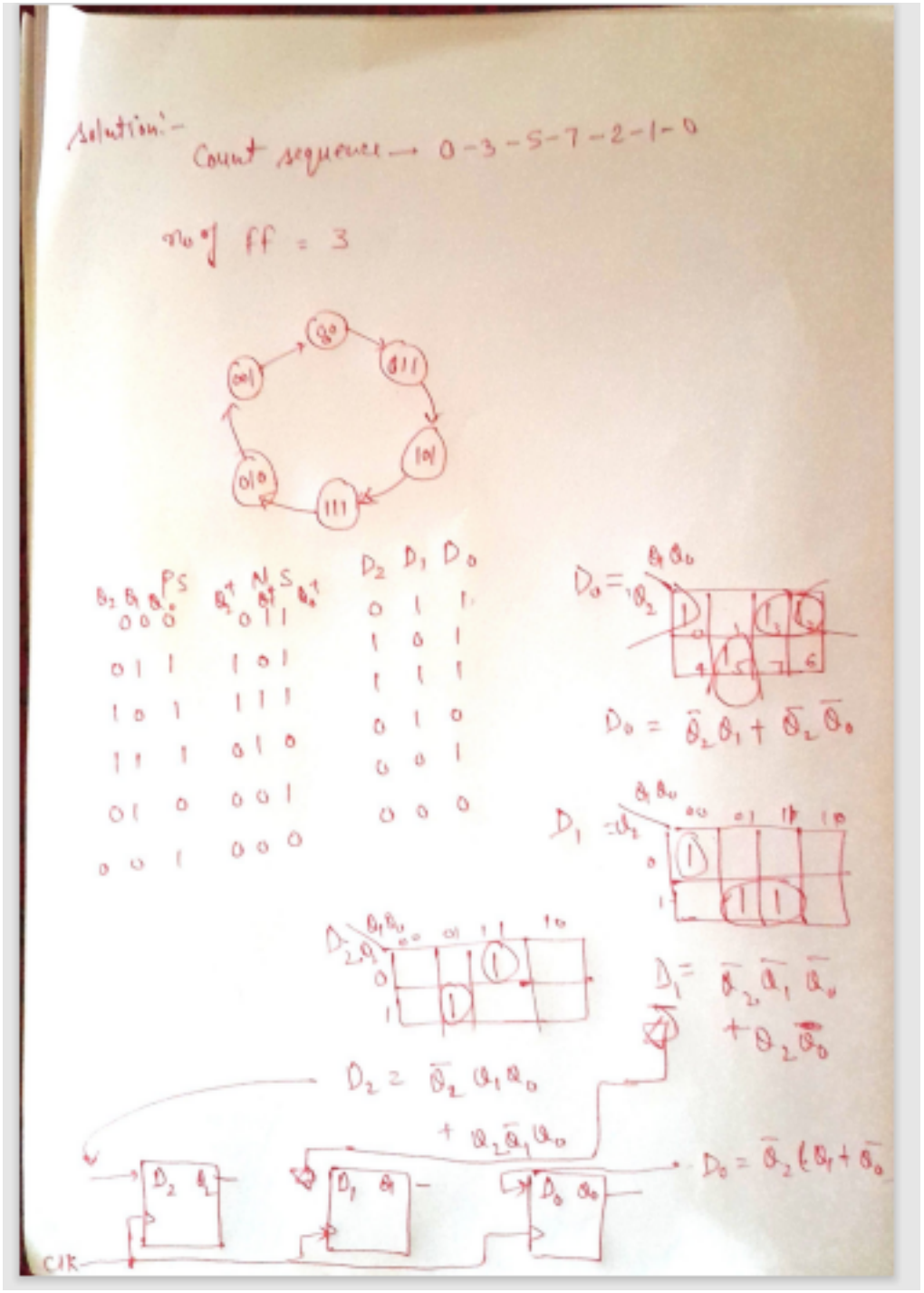


3.	A new clocked X-Y flip-flop is defined with two inputs, X and Y in addition to the clocked input. The flip flop functions as follows: If XY=01, the flip flop state (Q) becomes 1 at the next clock pulse If XY=10, the flip flop state (Q) becomes 0 at the next clock pulse. If X=Y, the flip flop toggles its state (Q) at the next clock pulse. i. Provide the truth table for the X-Y flip flop ii. Provide the characteristics table iii. Provide the Excitation table for the X-Y flip flop iv. Implement X-Y flip flop using a J-K flip flop v. Write the Verilog code for final implemented circuit using behavioral modeling.	**10**





4.	Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change. **Solution**: First stage of register:  	**10**
5.	Design a synchronous counter for the count sequence 0-3-5-7-2-1-0 using positive edge triggered D flip-flop. Write the Verilog code for the designed flip flop.	**10**



NOTE*: Please refer below to the BL – Bloom's Taxonomy Levels and mention the respective

level in the questions.

Bloom's Taxonomy Levels	Category
BL1	Remembering
BL2	Understanding
BL3	Applying
BL4	Analyzing
BL5	Evaluating
BL6	Creating