

Question Format & QP Setter Information

Name of Examination	Final Assessment Test, Winter 2022-23 Semester, (APRIL 2023)
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General Instructions (if any):

Q. No.	Sub-division	Question Text	Marks	Unit / Module No.	Difficulty Level E/A/T	BL	CO														
Answer All Questions			Total Marks: 10 X 10 = 100 Marks																		
1.		Implement the following function $F(x, y, z) = (1, 2, 3, 4, 5, 7)$ using (a) NAND gates only (b) NOR gates only	10	1	E	1	1														
2.		(a) Determine the minimized SOP and POS for $F(A, B, C, D) = \sum m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \sum d(0, 2, 14)$ using k-map. (b) Convert the following expression in canonical POS form $F(A,B,C) = A$	8 2	1	E	2	1														
3.		(a) Draw the circuit diagram for 4 x 1 multiplexer and write structural Verilog code for the same. (b) Write behavioral Verilog code D flip flop along with test bench.	5 5	2	A	2	2														
4.		Design a four-input priority encoder with input D1 having the highest priority, D0 having the next lower priority, D2 has the next lower priority and input D3 the lowest priority. Write the corresponding Verilog HDL code.	10	3	A	3	3														
5.		Design a 1 x 8 demultiplexer circuit using 1 x 4 demultiplexers and implement the full adder logic using the same.	10	3	T	3	3														
6.		Identify a suitable algorithm to multiply two n-bit signed binary numbers. Discuss the step-by-step process involved in multiplying the binary equivalent of 5×-6 using this algorithm.	10	4	A	4	3														
7.		Design a T flip flop using SR flip flop and write Verilog code for the same using behavioural modelling.	10	5	A	3	4														
8.		Design a synchronous counter for the given sequence using D – FF $3 \rightarrow 7 \rightarrow 0 \rightarrow 6 \rightarrow 4 \rightarrow 1$	10	5	E	3	4														
9.		Highlight the output sequence ‘Y’ that detects the occurrence of 101 for the following input sequence ‘X’ for a) Overlapping and b) Non-Overlapping case. Design an appropriate state table and the corresponding state diagram for both the conditions. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>X</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td> </tr> </table>	X	0	1	1	0	1	0	1	0	1	1	0	0	1	10	6	T	4	5
X	0	1	1	0	1	0	1	0	1	1	0	0	1								
10.		Design an Excess-3-to-BCD code converter using (a) PLA and (b) PAL	10	7	A	2	6														