VIT
Vellore Institute of Technology

Final Assessment Test – November/December 2023

Course: BECE102L - Digital Systems Design

Class NBR(s): 2275 / 2277 / 2279 / 2281 / 2283 / 2285 Slot: F1+TF1

Time: Three Hours Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Using the theorems of switching algebra, simplify the following functions:

   i) $F(A,B,C) = (A'+B)(A+B+C)C'$

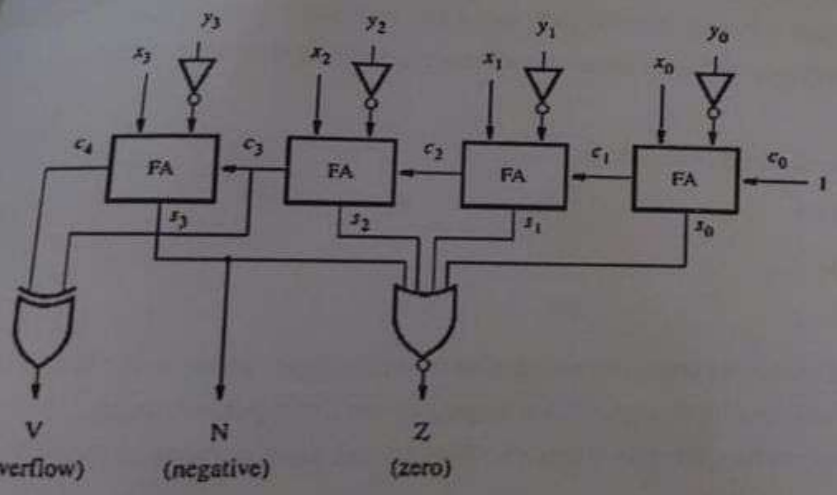
   ii) $F(A,B,C,D) = A\overline{B}C + B + B\overline{D} + AB\overline{D} + \overline{A}C$

2. Minimize the following function using K-map to identify the minimum SOP and POS expressions. Implement the minimal SOP and POS expressions using NAND and NOR gates respectively.

$$Y(A,B,C,D) = \sum_m (0,1,3,5,6,7,13,14) + \sum_d (2,4,8,10)$$

3. Design a three input combinational circuit that implements a majority function and delivers a high output, when there are more number of '1's in the input than zeros. Construct the circuit to implement the function with AOI gates and write a dataflow Verilog code for the circuit developed.

Write a structural verilog code for the circuit shown below, which produces three outputs V, N and Z. Use the primitive modules wherever avialable. Define the FA module in dataflow modeling and instantiate FA module in the structural code.



5. Implement the following Boolean function with a 4 × 1 multiplexer and external gates.

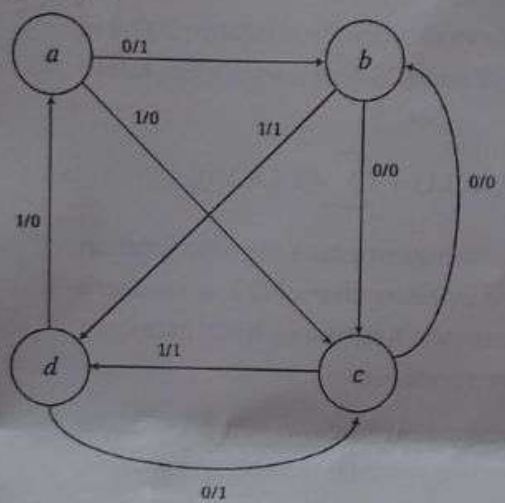
$F(A,B,C,D)=\sum m(1,2,5,7,8,10,11,13,15)$

Connect inputs B and C to the selection lines. The input requirements for the four data lines will be a function of variables A and D. These values are obtained by expressing F as a function of A and D for each of the four cases when BCs = 00, 01, 10 and 11. These functions may have to be implemented with external gates.

6. Use the Booth algorithm to multiply $(14)_{10}$ (multiplicand) by $(-5)_{10}$ (multiplier), and verify the result using binary multiplication. A clear explanation of every step of the algorithm is required.

7. Design the logic diagram of a 4-bit shift register with mode selection inputs S0 and S1. The register is operated according to the following: S0=S1=0: hold the current state, S0=1 and S1=0: performs shift left operation, S0=0 and S1=1 : load parallel input data, S0=S1=1 : the register is cleared. Write a behavioural Verilog code for the same.

8. Write a Verilog model of the FSM described by the state diagram as shown in Figure below.



9.(a) Design a Mealy FSM based sequence recogniser that has an input x and an output y. The circuit has to generate y=1, when the four values of x is 1001, otherwise y=0. Overlapping input pattern is allowed. Construct the circuit using T flipflops.

An example of the desired behavior is:

x: 0101 1111 0011 1

y: 0000 0000 0010 0

OR

9.(b) Design a Moore FSM based sequence recogniser that can detect either Pattern 101 or 011 and delivers a high output. Overlapping of the same pattern or both the patterns is also to be detected. Consider TFFS for the development of the circuit.

10. a) Differentiate PLA, PAL and PROM with reference to programmability. [5]

b) Describe about the generic architecture of FPGA, with a mention to LUT based Configurable logic blocks (CLB). [5]

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