VIT
Vellore Institute of Technology

Final Assessment Test – November/December 2023

Course: BECE102L - Digital Systems Design
Class NBR(s): 2276 / 2278 /2280 / 2282 / 2284 / 2286 Slot: F2+TF2
Time: Three Hours Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN "OFF" POSITION, IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions
(10 X 10 = 100 Marks)

1. i) Draw the CMOS circuit logic for the following Boolean function. [5]

$$F = \overline{AB + CD}$$

ii) Obtain the truth table of the following function, and express the function in sum-of-min terms and product-of-max terms form. [5]

$$bd' + acd' + ab'c + a'c'$$

2. Simplify the Boolean function F(w,x,y,z) = ∑(1,3,7,8,11,15) with don't care d(w,x,y,z) = ∑(0,2,5,9,10) and implement the logic circuit using AND-OR-INVERT gates.

3. Identify and debug the errors in the following Verilog code. Identify the circuit which represents this code and develop an equivalent gate level code for the same circuit.

```
module xx(p,q,r,s,t)
input  p,q;
output r,s,t;
reg r,s,t;
assign  r= (a==b);
assign s==(a>b);
assign t=(a<b);
endmodule;
```

4. a) Implement the following Boolean functions using 3:8 decoder [5]

$F_1 = \sum m\{1,2,8,9,15\}$,
$F_2 = \sum m\{1,3,4,9,13\}$,

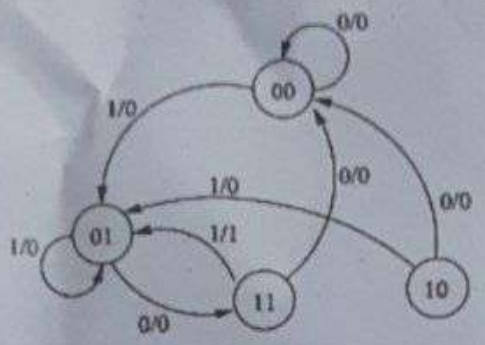
b) Write a gate level Verilog code for 2:4 decoder and also write test bench to verify it. [5]

5. Implement the following Boolean expression:
F = (wxy+w'x'y')z + z'(x'y + w'x) using single 4:1 multiplexer and necessary logic gates.
Utilize the inputs w and y as select lines of the multiplexer.

6. A logic circuit has two inputs X and Y each is a 2-bit unsigned number. It has an output Z which produces the product of two inputs.
a) What is the minimum number of bits required for the output number Z?
b) Design the circuit using only Half adders and external logic gates.
c) Write a structural Verilog code for the above circuit.

7. Design a modulo 8 up/down counter with control input.
Write a behavioural verilog code for the design.

8. Consider the following state diagram for a circuit with one input X and one output Z. Analyze this state diagram and draw its circuit implementation using JK flip-flops



9. a) Design a Moore Finite State Machine (FSM) system that detects the occurrence of the overlapping sequence 1011 using D flipflops. The system input X and output signals Y are given below:

X	0	1	0	1	1	0	1	1
Y	0	0	0	0	1	0	0	1

[OR]

9. b) Design a Mealy FSM with single input X. The output Y = 1, when either input sequence 101 or 110 has been detected on the input consecutively, otherwise Y = 0. Draw the state diagram, state table and develop circuit diagram using D flipflops.

10. a) Discuss the various applications of Programmable Logic Devices. [5]

b) Draw and explain about various steps involved in FPGA design flow. [5]