VIT

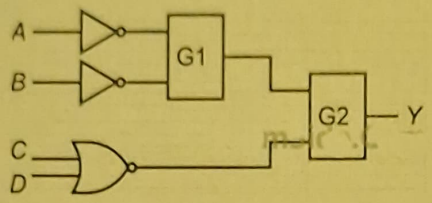
Vellore Institute of Technology

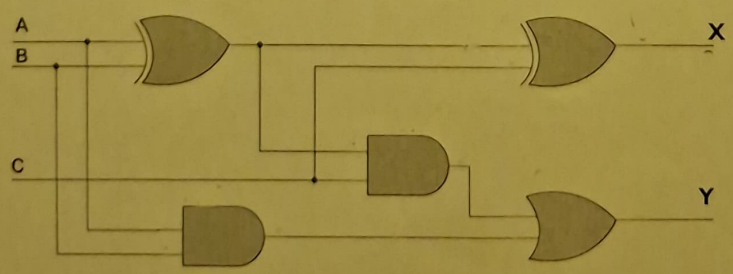
School of Electronics Engineering

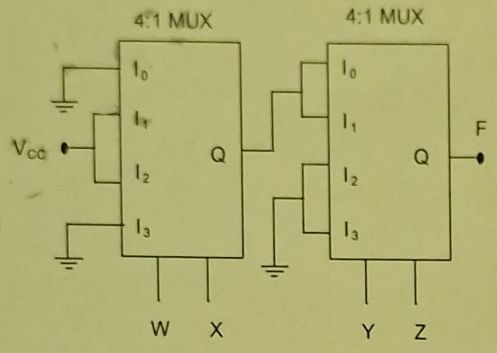
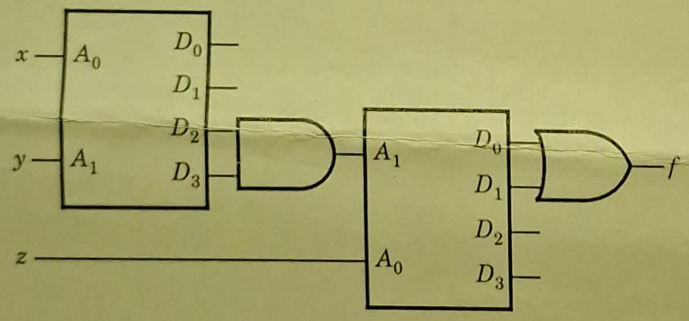
Winter Semester 2023-24 (MID Term-1)

Course Code : BECE102L
Course Name : Digital Systems Design
Faculty Name : Dr Sidharth Gautam

Exam Duration : 90 Minutes.
Slot: X11+X12+X21
Max. Marks: 50M

S. No	Questions	Max Marks	CO	BL
Q1	a) In the figure shown, identify the gates G1 and G2 for the output to be $Y = AB + \bar{C}\bar{D}$  b) Expand $A(\bar{A} + B)(\bar{A} + B + \bar{C})$ to maxterms and minterms	10 (5+5)	CO1	BL5
Q2	Simplify $F = \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D + B\bar{D} + B\bar{C}\bar{D}$ using Boolean algebra and postulates and implement the simplified expression using CMOS transistor logic by assuming that both the original and complemented version of each variable are available as gate input.	10	CO1	BL3

Q3	a) Execute the following verilog program for the given input a =4'b1010, b = 4'b1101 and compute the output.
	
	`module program(a,b,Y);`
	`input [3:0] a, b;`
	`output [4:0] Y;`
	`reg [4:0] Y;`
	`assign Y[0] = ~(a & b);`
	`assign Y[1] = (a[2] > b[0]) && ( a[3]< b[3]);`
	`assign Y[2] = (a !== b);`
	`assign Y[3] = (a != b) ? 1'b1 : 1'b0;`
	`assign Y[4] = a << 2) + (b >> 1);`
	`endmodule`
	
	b) Write a Verilog code in structural-level modelling for the following:
	 
		10
		(5+5)
			CO2	BL4

Q4	Design a combinational circuit with three inputs x, y, z, and three outputs A, B, C. When the binary input is 0, 1, 2, and 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, and 7, the binary output is two less than the input.	10	CO1	BL6
Q5	a) In the circuit shown, W and Y are MSBs of the control inputs. Write down the Boolean function F in SOP form.  b) Write down the Boolean function $f(x, y, z)$ represented in terms of a decoder.  	10 (5+5)	CO3	BL5