



VIT

Vellore Institute of Technology
(Declared on the University under section 3 of UGC Act, 1976)

Vellore – 632014, Tamil Nadu, India

SCHOOL OF ELECTRICAL ENGINEERING
FALL SEMESTER 2023-2024

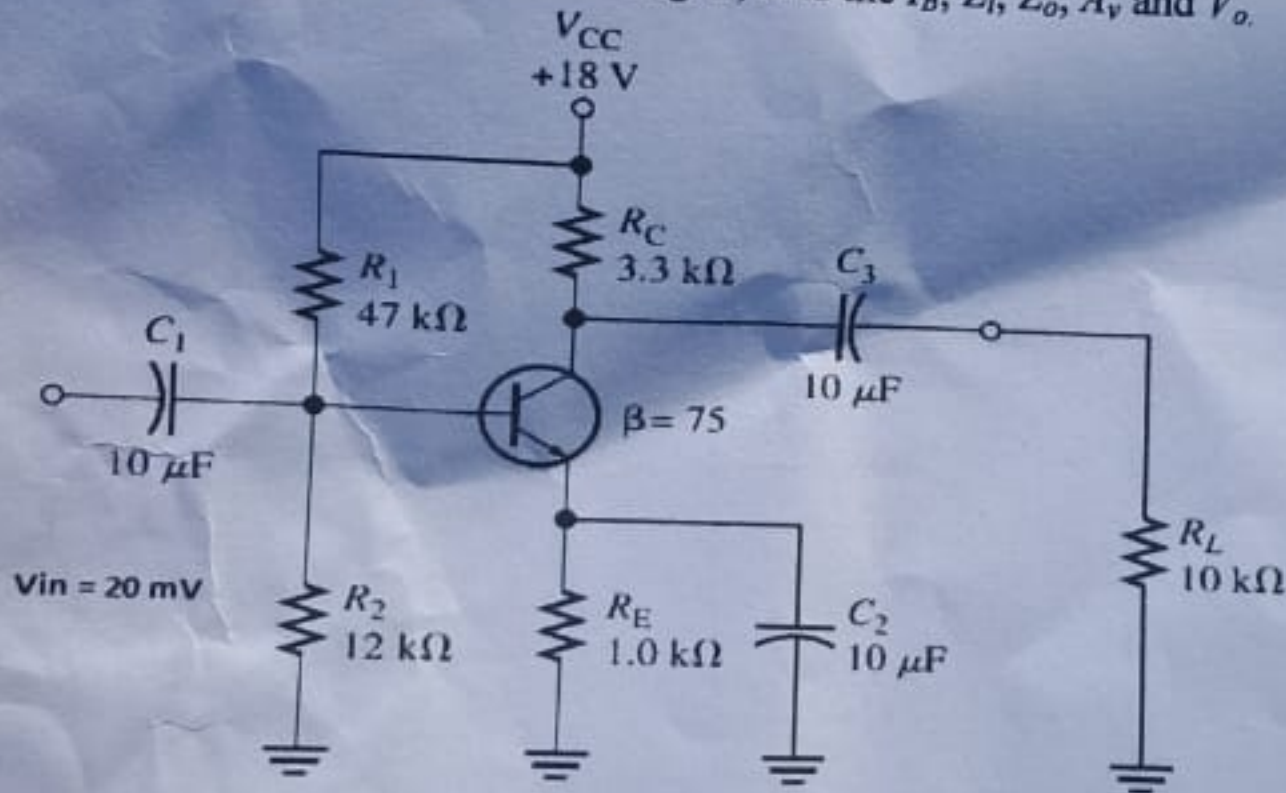
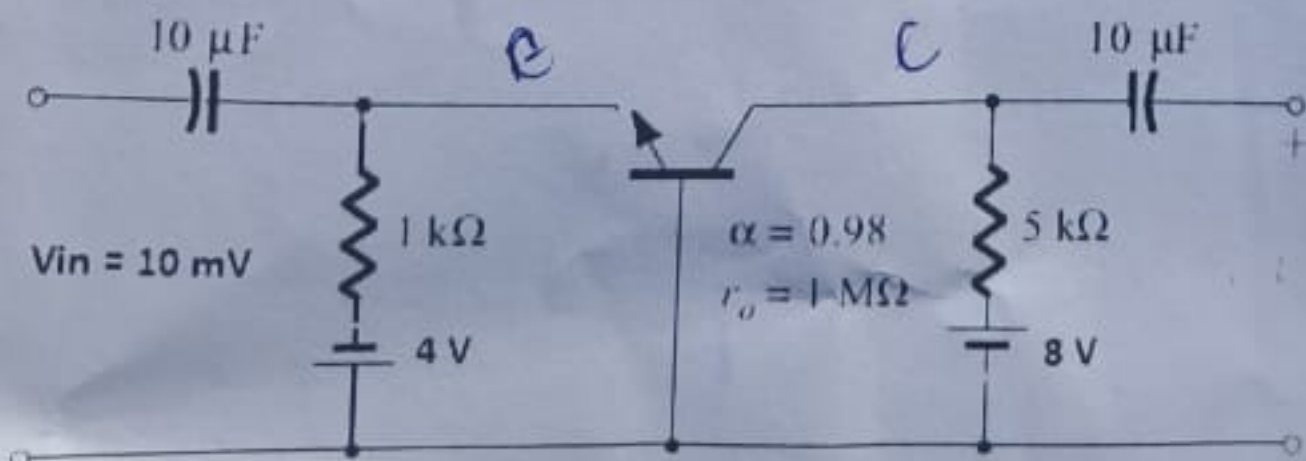
CAT-II

SLOT: A1

Programme Name & Branch : B.Tech & EEE and EIE Course Code: BEEE205L
Course Name : Electronic Devices and Circuits
Faculty Members : Dr. Venkataraman M.N, Dr. Sankardoss V
Class Number(s) : 1252, 8434
Date of the Examination : 13-10-2024, AN
Duration : 90 minutes

Max. Marks : 50

General instruction(s): Answer ALL Questions

Q. No.	Question	Marks	CO	BL
1.	For the following circuit as shown in Fig. 1, find the I_B, Z_i, Z_o, A_v and V_o.  Fig. 1	[10]	2	L4
2.	With the help of neat sketches, explain the construction, working and characteristics of the n-channel EMOSFET.	[10]	2	L2
3.	For the following circuit as shown in Fig. 2, find the I_B, Z_i, Z_o, A_v and V_o.  Fig. 2	[10]	2	L4



4.

For the circuit shown in Fig. 3, which uses an n-channel enhancement MOSFET, the transistor parameters are $V_{TN} = 0.8 \text{ V}$ and $K_n = 0.5 \text{ mA/V}^2$. Find V_{GS} , V_{DS} , I_D and region of operation of the transistor.

[10]

2

L3

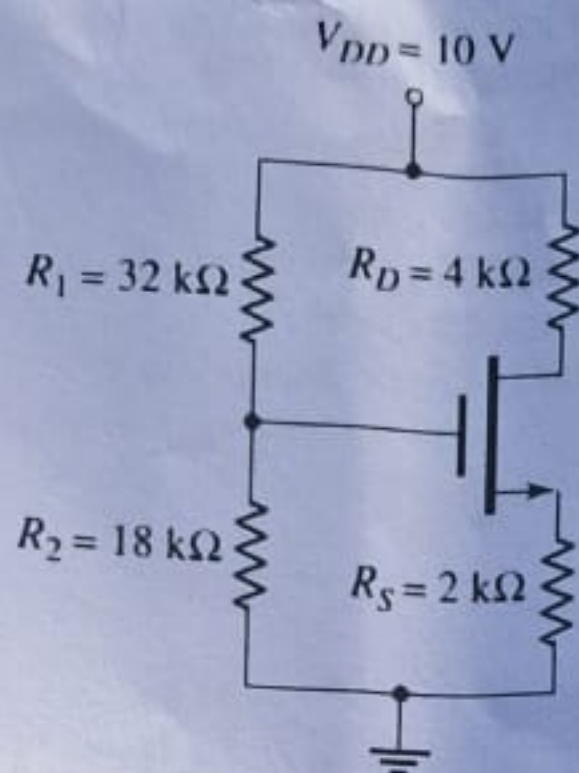


Fig. 3

5.

For the following circuit shown in Fig. 4. The circuit parameters are $V_{DD} = 12 \text{ V}$, $R_1 = 162 \text{ k}\Omega$, $R_2 = 463 \text{ k}\Omega$, $R_S = 0.75 \text{ k}\Omega$ and the transistor parameters are $V_{TN} = 1.5 \text{ V}$, $K_n = 4 \text{ mA/V}^2$. Find I_D , V_{DS} and V_{GS} .

[10]

2

L3

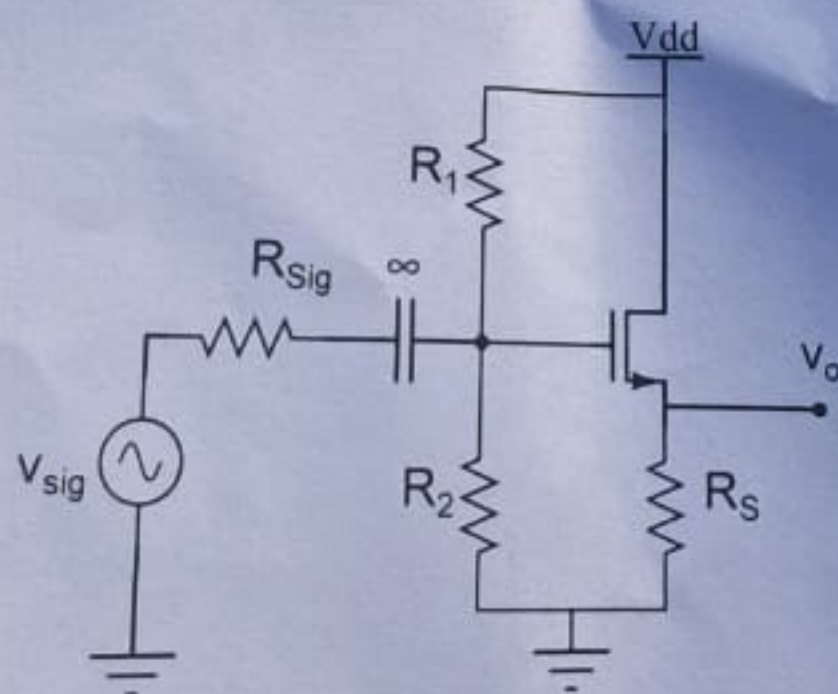


Fig. 4

