VIT
Vellore Institute of Technology

School of Electronics Engineering

Winter Semester 2023-24 Continuous Assessment Test – I

Programme Name & Branch: B. Tech (School of Computer Science Engineering)

SLOT: C2+TC2

Course Name & Code: Microprocessors and Microcontrollers BECE204L

Exam Duration: 90 Min. **Maximum Marks:** 50

Q. No.	Questions	Max Marks
1	a) Compare i3, i5 and i7 processors in terms of cores, frequency, multi-threading, turbo boost, etc.	5

	b) Identify and rectify (if any) the errors of the following instructions
	
	ADD B, R5
	SETB P1
	MOVC PC, #0523
	PUSH R3
	MOVC @A+PC, A
		5

2	Calculate the amount of delay caused by the below ALP program. Assume the crystal frequency is given as 11.059 MHz and the number of machine cycles are provided in parentheses. DELAY: MOV R0, #10100111B (1) AGAIN: MOV R7, #19H (1) HERE: MOV R2, #02 (1) BACK: NOP (1) NOP (1) NOP (1) DJNZ R2, BACK (2) DJNZ R7, HERE (2) DJNZ R0, AGAIN (2) RET (2)	10
3	Write an 8051 ALP to add ten numbers saved in the code memory from the location 200H onwards and store the result in R6 and R5. Where R5 holds the lower 8-bits of the result.	10
4	Write an 8051 program to get the length (8-bit number) and breadth (8-bit number) of a rectangle from port P0 and P1 respectively. Calculate area and perimeter of the rectangle and send them through port P2 and P3 respectively. Note: assume values of the inputs are such that the outputs do not exceed 8-bits	10
5	Write an ALP for generating a clock pulse of frequency 2KHz on P1.2 by using Timer 0 Mode 1. Provide necessary calculation.	10

Winter Semester 2023-24 Continuous Assessment Test – I Answer Key

C2+TC2

Microprocessors and Microcontrollers BECE204L

Q1 a) Compare i3, i5 and i7 processors in terms of cores, frequency, multi-threading, turbo boost, etc.

Ans. **i3:**

Cores: Typically, dual-core or quad-core.
Frequency: Moderately clocked, generally lower than i5 and i7 and varies from 2.93 GHz to 3.5 GHz
Multi-threading: Some i3 processors support hyper-threading, allowing for better multitasking performance.
Turbo Boost: Generally, i3 processors may not have Turbo Boost technology or have a limited version.

i5:

Cores: Usually quad-core, but some models may have six cores or more.
Frequency: Moderately to high clock speeds and varies from 2.40 GHz to 3.60 GHz.
Multi-threading: Most i5 processors support hyper-threading, providing better parallel processing capabilities.
Turbo Boost: i5 processors often feature Intel Turbo Boost technology, which dynamically increases the clock speed for better performance when needed.

i7:

Cores: Quad-core or higher, with some models having six or eight cores.
Frequency: Generally higher clock speeds compared to i5 and varies from 2.66 GHz to 5.4 GHz.
Multi-threading: Almost all i7 processors support hyper-threading, enabling efficient multitasking and parallel processing.
Turbo Boost: i7 processors typically feature Intel Turbo Boost technology, allowing for dynamic adjustments to clock speeds based on workload and thermal conditions.

Q1 b) Identify and rectify (if any) the errors of the following instructions.

Ans. ADD B, R5 - this instruction is wrong and can be rectified as ADD A, R5
SETB P1 - this instruction is wrong and can be rectified as MOV P1, #0FFH
MOVC PC, #0523 - this instruction is wrong and can be rectified as MOV PC, #0523
PUSH R3 - this instruction is wrong and can be rectified as PUSH 03.
MOVC @A+PC, A - this instruction is correct.

Q2 Calculate the amount of delay caused by the below ALP program. Assume the crystal frequency is given as 11.059 MHz and the number of machine cycles are provided in parentheses.

```
DELAY:
MOV R0, #10100111B (1)
AGAIN: MOV R7, #19H (1)
HERE: MOV R2, #02 (1)
BACK: NOP (1)
NOP (1)
NOP (1)
DJNZ R2, BACK (2)
DJNZ R7, HERE (2)
DJNZ R0, AGAIN (2)
RET (2)
```

Ans. Delay = 1.085 μs x (1+ 167 + (25 x 167) + 3(2x25x167) + 2((2x25x167)+(25x167) +167) + 2 = 59435.213 μs = 59.4 ms

Q3 Write an 8051 ALP to add ten numbers saved in the code memory from the location 200H onwards and store the result in R6 and R5. Where R5 holds the lower 8-bits of the result.

Ans.
```
ORG 00H
MOV DPTR, #200H
MOV R0, #10
LOOP:
CLR A
MOVC A, @A+DPTR
ADD A, R5
JNC H
INC R6
H: MOV R5, A
INC DPTR
DJNZ R0, LOOP

ORG 200H
DB: 00H, 10H, 20H, 30H, 40H, 50H, 60H, 70H, 80H, 90H
END
```

Q4 Write an 8051 program to get the length (8-bit number) and breadth (8-bit number) of a rectangle from port P0 and P1 respectively. Calculate area and perimeter of the rectangle and send them through port P2 and P3 respectively. Note: assume values of the inputs are such that the outputs do not exceed 8-bits.

Ans.
```
ORG 00H
MOV A, #0FFH
MOV P0, A
MOV P1, A
LOOP:
```

```
MOV A, P0          //LENGTH
MOV B, P1          //BREADTH
MUL AB             //AREA = LENGTH X BREADTH
MOV P2, A
MOV A, P0          //LENGTH
MOV B, P1          //BREADTH
ADD A, B           //(LENGTH + BREADTH)
MOV B, #2
MUL AB             //PERIMETER = 2(LENGTH + BREADTH)
MOV P3, A
SJMP LOOP
END
```

Q5 Write an ALP for generating a clock pulse of frequency 2KHz on P1.2 by using Timer 0 Mode 1. Provide necessary calculation.

Ans. XTAL = 11.0592 MHz
Clock pulse frequency= 2 KHz
Clock pulse time= 500 μs
Pulse width = 250 μs
250 μs/1.085 μs = 230.4 = 230

65536-230 = 65306 = FE1A H

```
ORG 00H
MOV TMOD, #01H
LOOP:
MOV TH0, #0FFH
MOV TL0, #1AH
CPL P1.2
SETB TR0
H: JNB TF0, H
CLR TR0
CLR TF0
SJMP LOOP
END
```