VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science Engineering

Winter Semester 2023-2024

Continuous Assessment Test – I

Program Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE204L Microprocessors and Microcontrollers

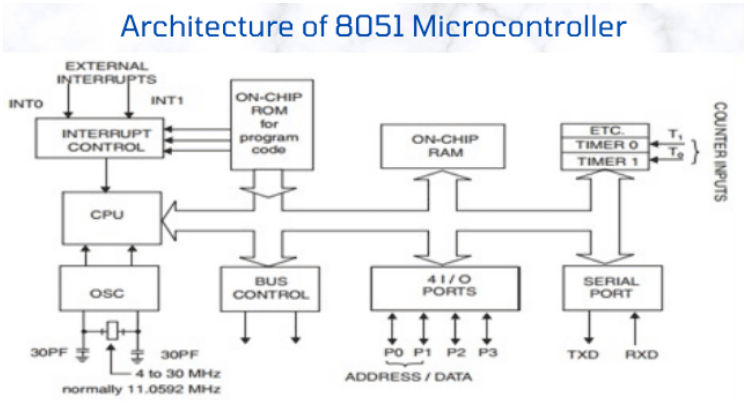
Slot: F1+TF1

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all the questions

<table>
<tr><th>S. No</th><th>Question</th><th>Marks</th></tr>
<tr><td>1. A</td><td>Draw the internal architecture of 8051 with a neat sketch

Answer:
 
</td><td>5</td></tr>
<tr><td>1. B</td><td>Identify if the following 8051 instruction have any error, if so give the correct instructions

Answer:

<table>
<tr><td>Given Instruction</td><td>Correct Instruction</td><td>Comments</td></tr>
<tr><td>DIV A,B</td><td>DIV AB</td><td>No comma</td></tr>
<tr><td>CPL A</td><td>CPL A</td><td>-</td></tr>
<tr><td>PUSH R0</td><td>PUSH 00H</td><td>Only direct address</td></tr>
<tr><td>ORL A, #25H</td><td>ORL A, #25H</td><td>-</td></tr>
<tr><td>MOV R2, R1</td><td>MOV R2, 01h
OR
MOV 02H,R1
OR
MOV 02H,01H</td><td>Not allowed</td></tr>
</table></td><td>5</td></tr>
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2	Analyze the following 8051 assembly program and show the stack and stack pointer during the execution of the program. The address of Bank0 = 00 t0 07H, Bank1 = 08 to 0FH, Bank2 = 10 to 17H and Bank3 = 18 to 1FH. Assume the default stack area. Answer: **Line No / Instruction / SP Address / SP Data / Line No / Instruction / SP Address / SP Data** 1 SETB PSW.3 — **Bank 1** 2 MOV R6, #25H — **0EH** — **25H** 3 MOV R7,#12H — **0FH** — **12H** 4 SETB PSW.4 — **Bank 2** 5 CLR PSW.3 6 MOV R1,#0F3H — **11H** — **0F3H** 7 MOV R2,#0DEH — **12H** — **0DEH** 8 MOV R3.#0FFH — **13H** — **0FFH** 9 PUSH 12H — **08H** — **0DEH** 10 PUSH 11H — **09H** — **0F3H** 11 PUSH 10H — **0AH** — **XXH** 12 PUSH 0FH — **0BH** — **12H** 13 PUSH 0EH — **0CH** — **25H** 14 POP 0DH — **0DH** — **25H** 15 POP 0CH — **0CH** — **12H** 16 POP 0BH — **0BH** — **XXH** 17 POP 0AH — **0AH** — **0F3** 18 END	10
3	Assume in the 8051 ROM locations 3000H – 3009H have the values 20H, 31H, 42H, 51H, 62H, 70H, 80H, 90H, 0A1H, and 0B2H respectively. Write an assembly program to perform addition of these ten numbers. Store the carry at 70H and Sum at 71H of RAM. Also write the expected data stored at 70H and 71H of RAM. **Answer:** **ORG 3000H** **DB 20H,31H,42H,51H,62H,70H,80H,90H,0A1H,0B2H** **ORG 0000H** **MOV DPTR,#3000h** **MOV R0, #00H** **MOV R1,#0AH** **MOV R2,#00H** **Loop: CLR A** **MOVC A,@A+DPTR** **ADD A,R0** **JNC L1** **INC R2** **L1: MOV R0,A** **INC DPTR** **DJNZ R1,Loop** **MOV 71H,R0** **MOV 70H,R2** **END** **Carry is 04 and Sum is 19H** D:0x70: 04 19	10

4	Assume a switch is connected at port pin P1.2, monitor the status of the switch. If the status of the switch is HIGH ("1") then transfer data from R1 (Bank 0) to Port P3, else transfer data from R0 (Bank 0) to Port P3. **Answer:** **ORG 0000H** **CLR PSW.3** **CLR PSW.4** MOV R0,#0FH **// Not mandatory** MOV R1,#0F0H **// Not mandatory** **L2: JB P1.2, L1** MOV A,R0 // MOV P3,R0 Both are correct MOV P3,A **SJMP L2** **L1:** MOV A,R1 //MOV P3,R1 Both are correct MOV P3,A **SJMP L2** **END**	10
5	Write an 8051 assembly program to generate a 2ms waveform with 50% duty cycle (Square wave generator) on the port pin P1.5. Assume the clock frequency of 8051 is 12 MHz and use the timer T1. **Answer:** **ORG 0000H** **MOV TMOD,#01H** **Begin: MOV TH1,#0FCH //OFF TIME** **MOV TL1,#18H** **ACALL DELAY** **MOV TH1,#0FCH //ON TIME** **MOV TL1,#18H** **ACALL DELAY** **SJMP Begin** **DELAY:CPL P1.5** **SETB TR1** **L1:JNB TF1,L1** **CLR TF1** **CLR TR1** **RET** **END** **Note: We can use same ACALL DELAY for ON and OFF time of a signal because it is a square wave.**	10