Final Assessment Test – July 2023

VIT
Vellore Institute of Technology

Course: BECE303L - VLSI System Design
Class NBR(s): 0243 / 0245 / 0247 / 0249 / 0251 / 0253 / 0255 / 0257 / 0258 / 0260
Slot: A2+TA2

Time: Three Hours
Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN "OFF" POSITION IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions
(10 X 10 = 100 Marks)

1. a) An NMOS transistor, operating in the linear-resistance region with $V_{DS} = 0.1$ V, is found to conduct 60 μA for $V_{GS} = 2$ V and 160 μA for $V_{GS} = 4$ V. What is the apparent value of threshold voltage V_t?
   b) If $\mu_n C_{ox} = 50\ \mu A/V^2$, what is the device W/L ratio?
   c) If the device is operated at $V_{GS} = 3$ V, at what value of V_{DS} will the drain end of the MOSFET channel just reach pinch-off, and what is the corresponding drain current?

2. Write a short note on the following non-ideal effects
   a) Drain induced barrier lowering effect
   b) Body bias effect

3. Implement transmission gate based positive and negative edge triggered flip flop. Explain its operation with timing diagram.

4. Explain in detail the fabrication steps of P-well process.

5. Draw a stick diagram for the following OR-AND-INVERT logic and estimate the area for λ = 45nm

   $F = \overline{(A+B)\cdot(C+D)}$

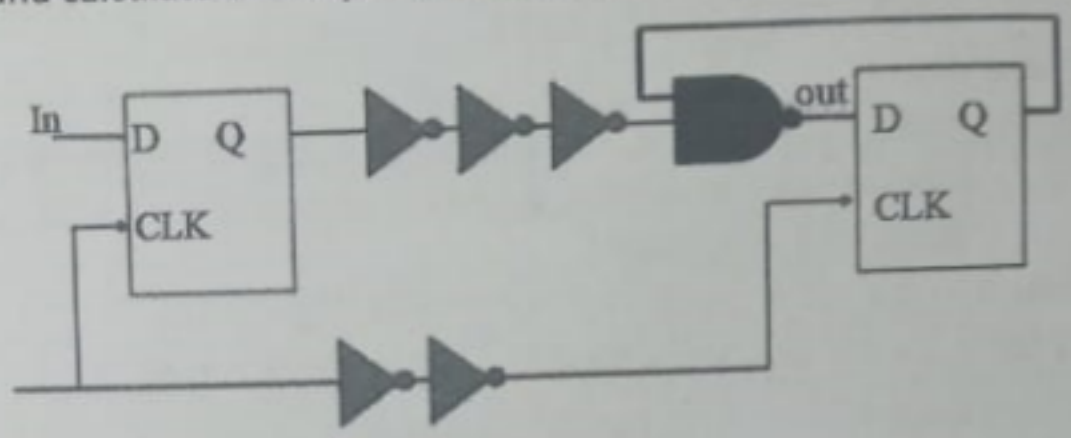
6. Implement a 4-input Majority gate using pass transistor logic. Assume Majority gate as a gate which generates output as '1' if the majority of the inputs are '1' else the output is'0'

7. a) Design a half adder using dynamic logic.
   b) Explain why cascading of dynamic gates is not possible with an example.

8. Consider a process in which pMOS transistors have three times the effective resistance as nMOS transistors. Implement the following function in this process and find worst case rise delay and fall delay.

   $Y = \overline{(A(B+C))+D}$

9. Consider the following circuit and given timing specifications to check whether there are any violations. If there is any violation vary the delay values accordingly and calculate the required minimum clock period.



Given timing specifications,

Tclock_Q1 = Tclock_Q2 = 2ns

Tsetup_time1 = Tsetup_time2 = 3ns

Thold_time1 = Thold_time2 = 6ns

The inverters have a delay of 1ns each and the NAND gate propagation delay is given as 2ns

10. What is a DRAM? What are its characteristics? List out the differences between DRAM and SRAM.

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