VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Winter Semester 2023-2024 Continuous Assessment Test – I

Programme Name &Branch: BCB, BCE, BCI, BCT, BDS, BKT **SLOT: D1+TD1**

Course Name & code: Computer Architecture and Organization- BCSE205L

Class Number (s): Common to all

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all five questions

Q.No.	Question	Max Marks
1.	**Scheme of evaluation:** Sl. No | Topic | Marks 1. | Assembly Code | 4 1. | Register flow of operations | 6 Write an Assembly language programming for the following expression using the IAS computer Instruction set and interpret the flow of the IAS computer (Register flow of operations). R = P – Q Assume the memory locations 800, 801, and 802 for P, Q, and R respectively. Ans: R = P – Q Assembly Code: 1. LOAD M[800] : AC ← M[800] 2. SUB M[801] : AC ← AC – M[801] 3. STORE M[802] : M[802] ← AC 4. HALT Register Flow of Operations	10

MAR ← PC
MBR ← M[MAR]
IBR ← MBR<20..39>
IR ← MBR<0..7>
MAR ← MBR<8..19>
MBR ← M[MAR]
AC ← MBR

1

IR ← IBR<0..7>
MAR ← IBR<8..19>
MBR ← M[MAR]
AC ← AC - MBR

2

PC ←PC+1
MAR ← PC
MBR ← M[MAR]
IBR ← MBR<20..39>
IR ← MBR<0..7>
MAR ← MBR<8..19>
MBR ← AC
M[MAR} ← MBR

3

IR ← IBR<0..7> 4

2.

Scheme of evaluation:

Sl. No	Topic	Marks
2.a	Booth recoded table	3
2.b	Steps	4
2.b	Description of each step	2
2.b	Final result	1

1

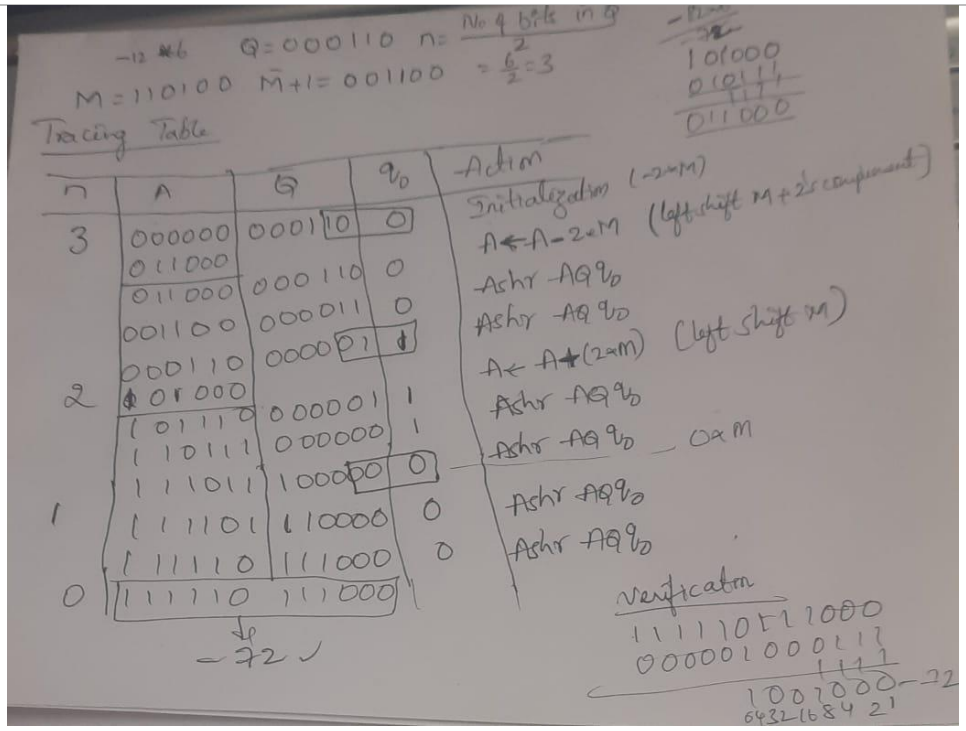
a. Show the Bit pair recoded table for three-bit combinations. 3 Marks.

Multiplier bit-pair		Multiplier bit on the right	Multiplicand selected at position i
$i+1$	i	$i-1$	
0	0	0	0 × M
0	0	1	+1 × M
0	1	0	+1 × M
0	1	1	+2 × M
1	0	0	−2 × M
1	0	1	−1 × M
1	1	0	−1 × M
1	1	1	0 × M

b. Perform the multiplication with the numbers -12 and 6 using the Modified Booth algorithm. A description of each step is required. (7 Marks)

Ans:

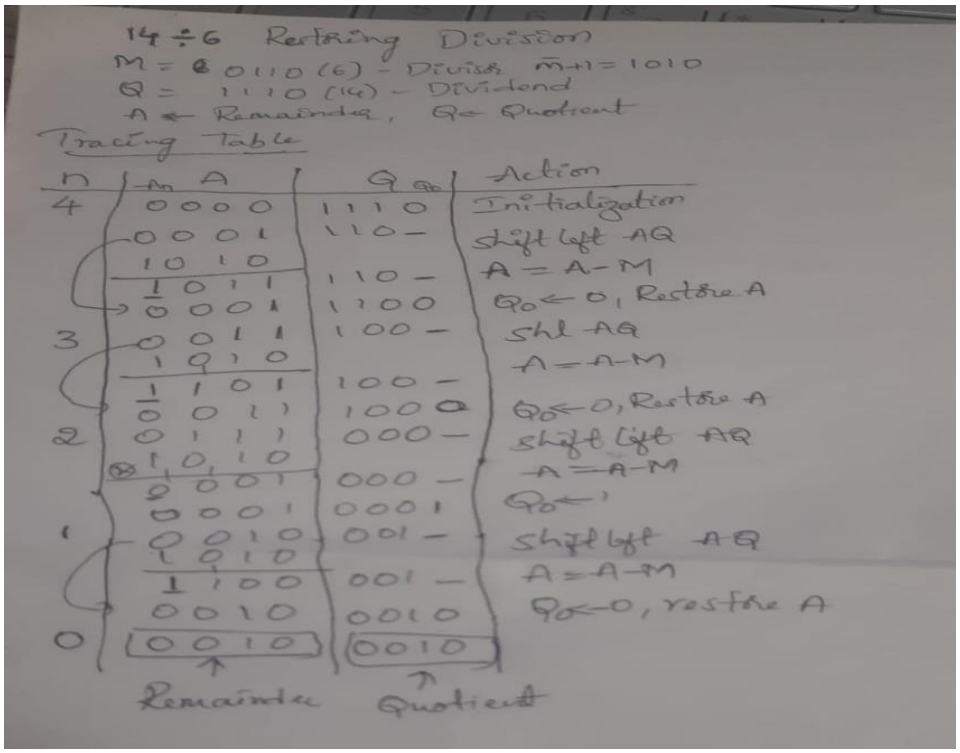
10
[3 + 7]



3.	**Scheme of evaluation:** **Sl. No** | **Topic** | **Marks** 3.a | Identification | 1 3.a. | Justification | 3 3.b | Steps | 4 3.b | Description of each step | 2 3.b | Final result | 1 a. Identify the most widely used signed number representation among the available representations. Justify your answer. 4 Marks Ans: 2's Complement Representation is most widely used for signed number representation. Other representations and their limitations are as follows. • Signed magnitude representation: – 2 representations for 0 – Simple – 255 different numbers can be represented. – Need to consider both sign and magnitude in arithmetic – Different logic for addition and subtraction • 1's complement representation: – 2 representations for 0 – Complexity in performing addition and subtraction – 255 different numbers can be represented. • 2's complement representation: – Only one representation for 0 – 256 different numbers can be represented. – Arithmetic works easily	10 [4 + 6]

b. Perform the division with the numbers 14 and 6 (ie. 14/6) using the restoring algorithm. A description of each step is required.
(7 Marks)

Ans:



4. **Scheme of evaluation:** 10 [5 + 5]

Sl. No	Topic	Marks
4.a	RISC vs CISC	5
4.b(i)	Binary Conversion	1
4.b(i)	Arithmetic Shift Right	1.5
4.b(ii)	Binary Conversion	1
4.b(ii)	Arithmetic Shift Right	1.5

a. Compare and Contrast RISC with CISC. (5 Marks)

Ans:

CISC	RISC
Emphasis on hardware	Emphasis on software
Includes multi-clock complex instructions	Single-clock, reduced instruction only
Memory-to-memory: "LOAD" and "STORE" incorporated in instructions	Register to register: "LOAD" and "STORE" are independent instructions
Small code sizes, high cycles per second	Low cycles per second, large code sizes
Transistors used for storing complex instructions	Spends more transistors on memory registers

b. Perform arithmetic shift right operations one time on the following decimal numbers. (i) 13 (ii) 27
Represent the above numbers in 8-bit binary form (5 Marks)

Ans:

13 in binary

0	0	0	0	1	1	0	1

Arithmetic Shift Right one time

0	0	0	0	0	1	1	0

27 in binary

0	0	0	1	1	0	1	1

Arithmetic Shift Right one time

0	0	0	0	1	1	0	1

5. **Scheme of evaluation:** 10 [4+6]

Sl. No	Topic	Marks
5(a)	3-address instruction format	2
5(a)	2-address instruction format	2
5(b)	List of addressing modes	2
5(b)	Explanation with example	4

(a) Evaluate the following expression in 3-address and 2-address instruction formats.

A = (B * C) + (D * E) (4 Marks)

Ans:

3-address instruction format

MUL R1, B, C
MUL R2, D, E
ADD A, R1, R2

2-address instruction format

MOV R1, B
MUL R1, C
MOV R2, D
MUL R2, E
ADD R1, R2
MOV A, R1

(b) Elucidate various addressing modes with examples. (6 Marks)

Ans:

- Implied Addressing Mode
- Immediate Addressing Mode
- Direct Addressing Mode
- Indirect Addressing Mode
- Register Direct Addressing Mode
- Register Indirect Addressing Mode
- Displacement Addressing Mode
  - Relative Addressing Mode
  - Indexed Addressing Mode
  - Base Addressing Mode
- Auto Increment and Auto Decrement Addressing Mode

Explanation

Basic Addressing Modes differences :

	Mode	Algorithm	Advantage	Disadvantage
1	Immediate	Operand=1	No memory Reference	Limited operand magnitude
2.	Direct	EA = A	Simple	Limited address space
3	Indirect	EA =(A)	Large Address space	Multiple Memory References
4.	Register	EA = R	No memory Reference	Limited address space
5.	Register Indirect	EA = (R)	Large address space	Extra memory space
6	Displacement	EA = A+(R)	Flexibility	Complexity
7.	Stack	EA= Top of Stack	No memory Reference	Limited Applicability