REG.NO.:

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

NAME OF THE SCHOOL
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2024-2025

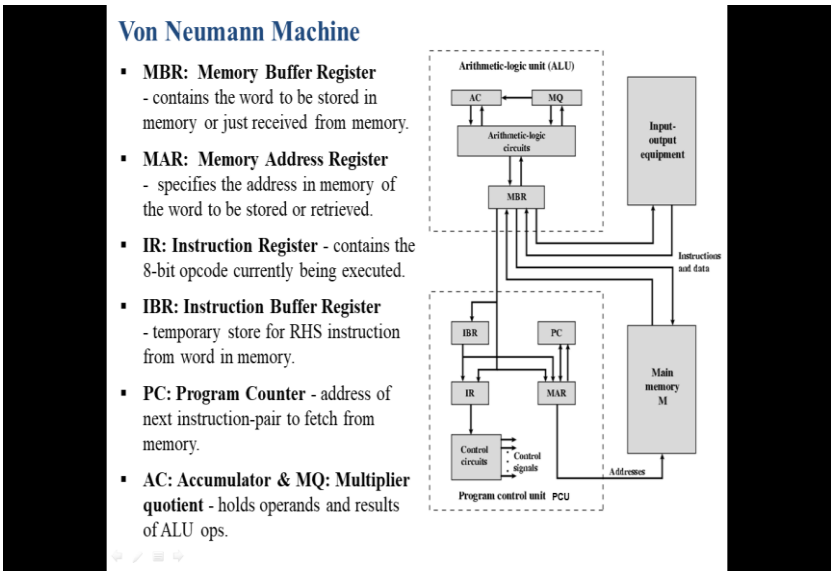
SLOT: C1 + TC1

Programme Name & Branch : B.Tech Computer Science and Engineering
Course Code and Course Name : BCSE205L and Computer Architecture and Organization

Q. No	Question	M	CO	BL
1.		7	CO1	1

Scheme of Evaluation		
Sl. No.	Topic	Marks
1	List of registers (6)	3
2	Brief Description on each	4
3	RISC Vs CISC (Min. 3 comparisons for each)	3

a. Explain the importance of different registers in the IAS computer and illustrate their interconnections with a neat block diagram.



		3		1

b. Compare CISC and RISC architecture.

RISC	CISC
It is a Reduced Instruction Set Computer.	It is a Complex Instruction Set Computer.
It focuses on Software.	It focuses on Hardware.
It uses only a Hardwired control unit.	It uses both hardwired and microprogrammed control units.
Transistors are used for more registers.	Transistors are used for storing complex instructions.
Code size is large.	Code size is small.
The uses of the pipeline are simple in RISC.	Uses of the pipeline are difficult in CISC.
An instruction is executed in a single clock cycle.	Instruction may take more than one clock cycle.
An instruction can fit in one word.	Instructions are larger than the size of one word.
The execution time of RISC is very short.	The execution time of CISC is longer.
The program written for RISC architecture needs to take more space in memory.	The Program written for CISC architecture tends to take less space in memory.

2.

Scheme of Evaluation		
Sl. No.	Topic	Marks
1	Program	4
2	Description	3
3	Memory Layout	3

Write an assembly code to execute the following operation and interpret to Von Neumann architecture

Z= ((A+B) + (C−D)) * E

Note: Program can be stored at memory location 300 onwards and Data variables are available from loation address 500 onwards.
Assembly Language : [5 marks]

1	LOAD M(500)	Acc←M[500]
2	ADD M(501)	Acc←Acc+M[501]
3	STORE M(505)	M[505]←Acc
4	LOAD M(502)	Acc←M[502]
5	SUB M(503)	Acc←Acc-M[503]
6	STORE M(506)	M[506]←Acc
7	LOAD M(505)	Acc←M[506]

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		8	ADD M(506) Acc←Acc+M[507]			
		9	STORE M(505) M[508]←Acc			
		10	LOAD MQ,M(505) MQ←M[508]			
		11	MUL M(504) Acc, MQ←M[504] x MQ			
		12	STORE M(505) M[509]←Acc			
		13	LOAD MQ Acc←MQ			
		14	STORE M(506) M[510]←Acc			

Memory Layout

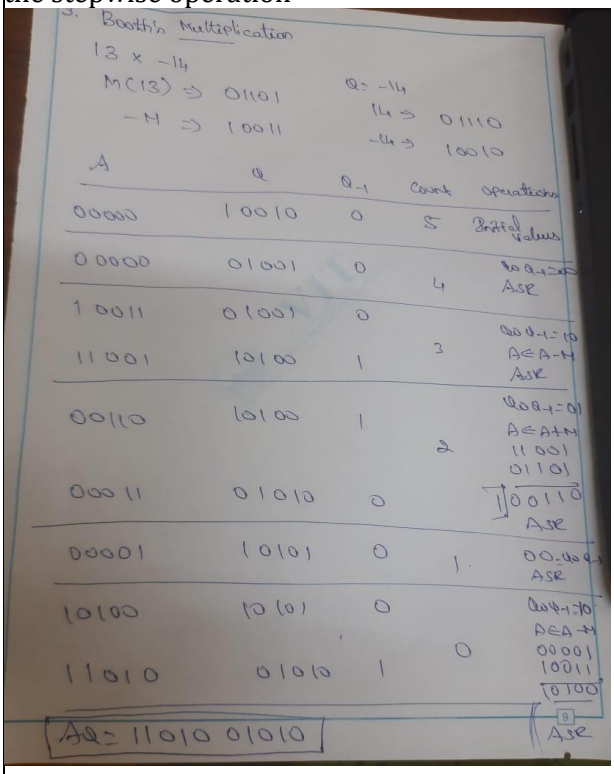
Instructions	300	1	2
	301	3	4
	302	5	6
	303	7	8
	304	9	10
	305	11	12
	306	13	14
		….	…
		….	…
		…	…
Data	500	A	
	501	B	
	502	C	
	503	D	
	504	E	
	505	Z	
	506	Z+1	

Register Transfer Notation [5 marks]

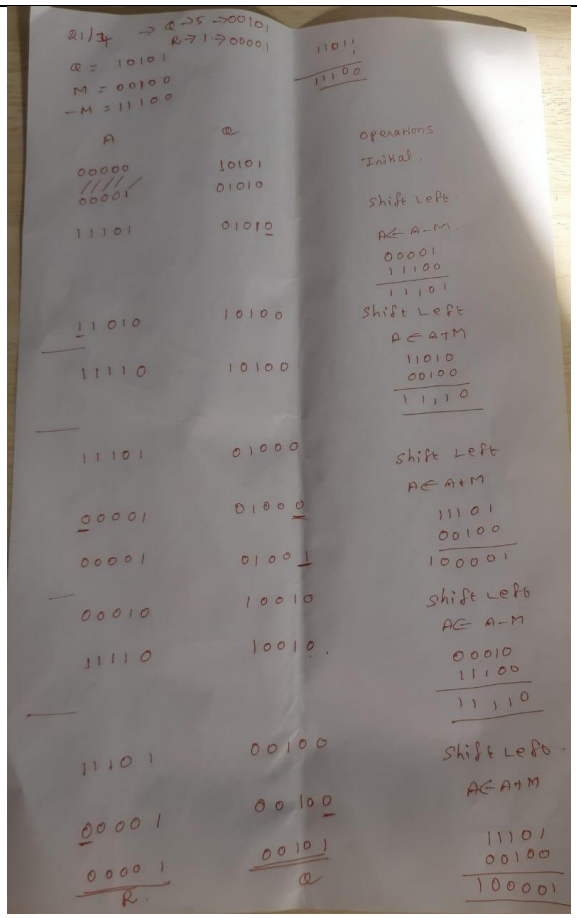
3.

Scheme of Evaluation		
Sl. No.	Topic	Marks
1	Algorithm/Flowchart	4
2	Table of steps	6

10 | CO1 | 3

	Calculate 13 X -14 using Booth's multiplication algorithm with explanation of the stepwise operation 			
4.	a) Perform non-restoring division with a dividend of 21 and a divisor of 4.	6	CO1	3

Scheme of Evaluation		
Sl. No.	Topic	Marks
1	Table of steps	6
2	Each standard 2 marks	4



b) Represent 12.25 in Single and Double Precision IEEE -754 standard.

Single Precision

0	10000010	10001000000000000000000

Double Precision

0	10000000010	10001000000000000000000000000000000000000000000000000000

4

5.

Scheme of Evaluation		
Sl. No.	Topic	Marks
1	3 categories	5
2	Based on operand references	5

CO1

3

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Discuss in detail the classification of instructions based on operations performed and number of operand references with suitable example.

a. Based on operation[5 marks]

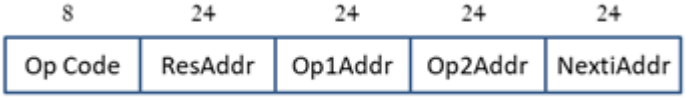
- Data Movement
  Memory : LOAD, STORE, MOV
  I\O Instructions: IN, OUT

- Data Processing
  Arithmetic : Add, Sub, MUL
  Logic Instructions: AND, OR

- Control Instructions
  Conditional : JNZ, JZ
  Un Conditional: Jump

b. Based on operand references[5 marks]

- 4 Address Instruction

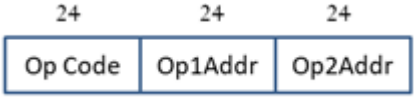


  Example: add M1,M2,M3, nexti

- 3 Address Instruction

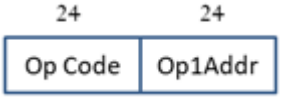
  Example: add M1,M2,M3

- 2 Address Instruction



  Example: add M2,M3

- 1 Address Instruction



  Example: add M2

- 0 Address Instruction
  PUSH, POP

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