REG.NO.: 24BEC0057

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2024-2025

SLOT: C1 +TC1+TCC1

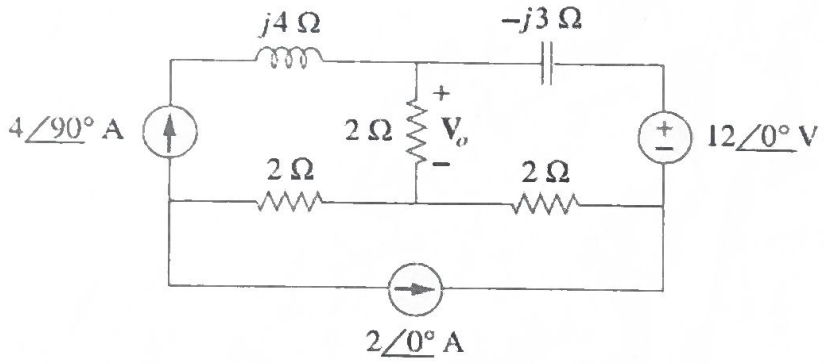
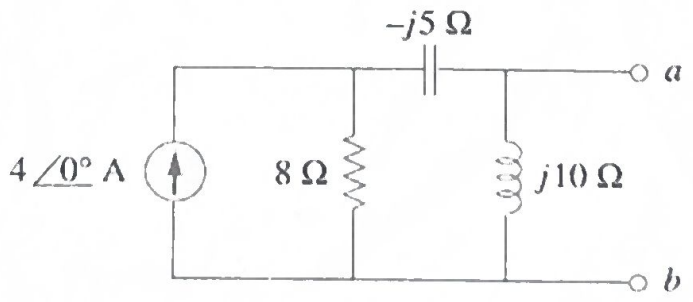
Programme Name & Branch	**: B. Tech / ECE / BML / BVD**
Course Code and Course Name	**: BECE203L – Circuit Theory**
Faculty Name(s)	**: Dr. Sathya P, Dr. Dr.Velmurugan V, Dr.Venugopal P, Dr.Vaegae Naveen Kumar, Dr.Kumaravel S, Dr. Avinash Chandra, Dr.Abdul Majeed K**
Class Number(s)	**: VL2024250500734, 0736, 0728, 0724, 0737, 0739, 0727, 0731**
Date of Examination	**: 29.01.25**
Exam Duration	**: 90 minutes**

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:

CO1: Apply the knowledge of various circuit analysis techniques such as mesh analysis, nodal analysis, and network theorems to investigate the given network.
CO2: Analyse the resonance and transient response of the first order, second order circuits.
CO3: Able to solve the networks using graphical approach.

Q. No	Question	M	CO	BL
1.	Compute V_o in Fig. (a) using mesh analysis.  Fig. (a)	10	1	3
2.	Construct both the Thevenin's and Norton's equivalent circuit at the terminals a-b in Fig. (b).  Fig. (b)	10	1	3

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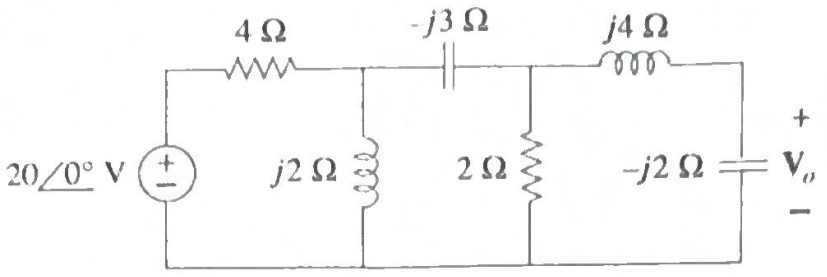
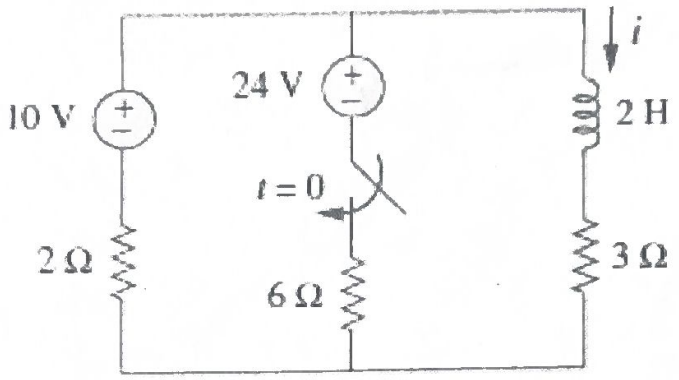
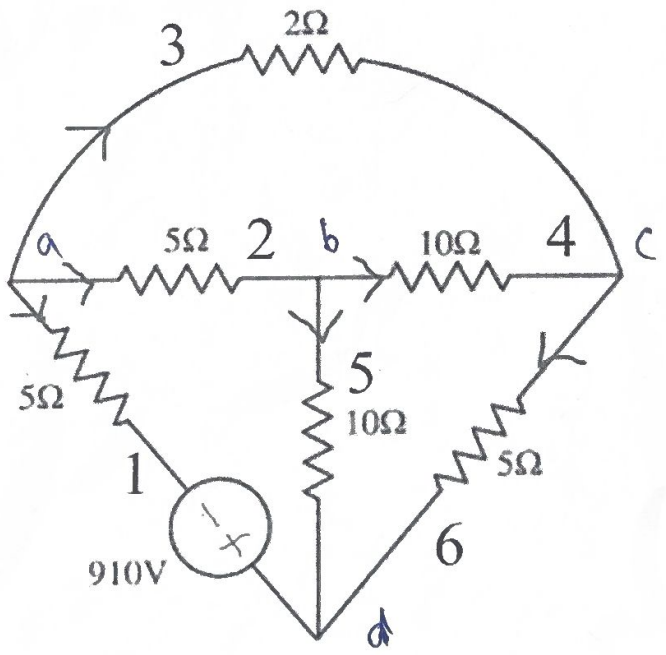
3.	Apply the concept of source transformation to find V_o in Fig. (c).  Fig. (c)	10	1	3
4.	Calculate the inductor current i(t) for t>0 of the circuit shown in Fig. (d)  Fig. (d)	10	2	3
5.	Construct a network graph for given the circuit diagram as shown Fig. (e) . Find the incidence matrix and for a tree consisting of (1, 5, 6) (i) draw tie set matrix (ii) draw cut-set matrix.  Fig. (e)	10	3	3