REG.NO.:

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SLOT: D1

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

Programme Name & Branch	**: B. Tech & Electronics and Communication**
Course Code and Course Name	**: BECE406E and FPGA Based System Design**
Faculty Name(s)	**: Antony Xavier Glittas X**
Class Number(s)	**: VL2024250500726**
Date of Examination	**: 30/01/2025**
Exam Duration	**: 90 minutes**

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)
  1. Understand architectures of programmable logic devices
  2. Understand various abstraction level in Verilog HDL
  3. Construct high-speed arithmetic and memory circuits

Q. No	Question	M
Q1	Describe how the Apex-2 logical element works in normal mode and counter modes with the necessary diagrams.	10
Q2	Implement the Boolean expression F(A,B,C,D)= ∑m(1,2,7,9,10,11,13,15) using PLA which has 6 input lines and three 2-input OR gates.	10
Q3	Write a Verilog code and test bench to add two 4-bit numbers using a single full adder in multiple cycles and provide the necessary circuit diagram.	10
Q4	Describe the architectures with a suitable diagram of the carry-lookahead adder and carry-save adder and compare their performances.	10

Q5	i) Identify the errors and correct them (if any).
	a. module first(input a, b, c, output reg d);
	b. 8'd-5;
	c. {c,d} <= a>>3;
	d. a = {4{1'b1},c};
	e. reg [3:0]x,y,z; assign z = x-y;
	ii) write a Verilog code to implement a 4-bit carry select adder in dataflow style.
		10

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