Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

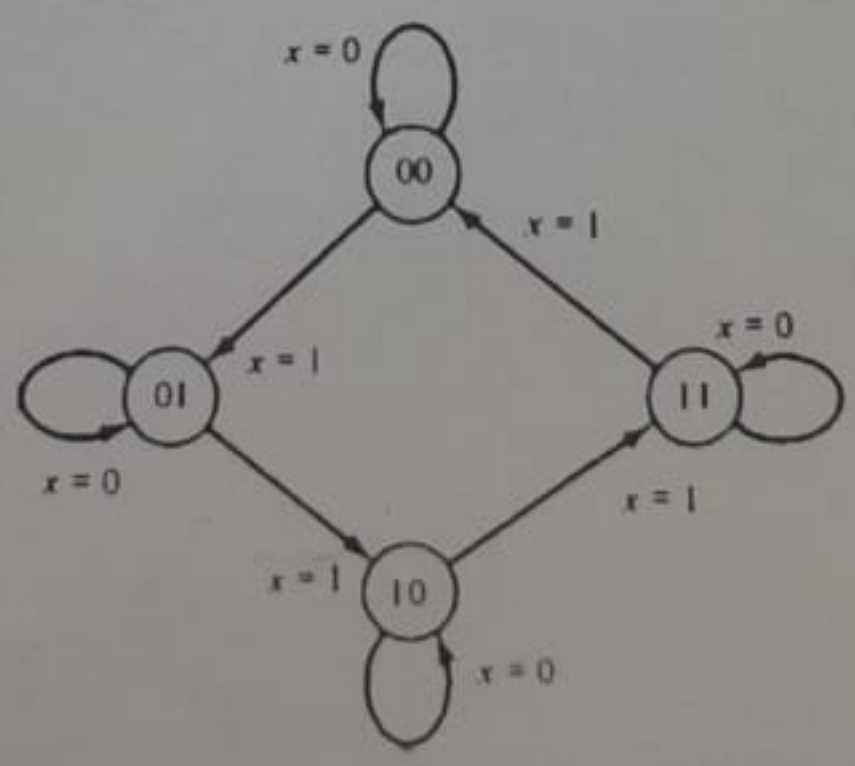
SCHOOL OF ELECTRICAL ENGINEERING (SELECT)
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2024-2025

SLOT: C2+TC2

Programme Name & Branch : B.Tech (EEE, EIE & BEL)
Course Code and Course Name : BEEE206L and Digital Electronics
Faculty Name(s) : Vijayakumar D
Class Number(s) : 0102931
Date of Examination : 15th October 2024
Exam Duration : 90 minutes **Maximum Marks: 50**

General instruction(s):

- Answer All Questions

Q. No	Question	M
1.	A device which is a combinational circuit that uses single input (1 port) that can be directed throughout several outputs (8 ports) design and write a Verilog code using behavioural level of modelling.	10
2.	Design a sequential circuit using T flip flops and state diagram from the given state transition table.	10
3.	Design a 2 bit binary counter using JK – flip flops, the state diagram shown below. 	10

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

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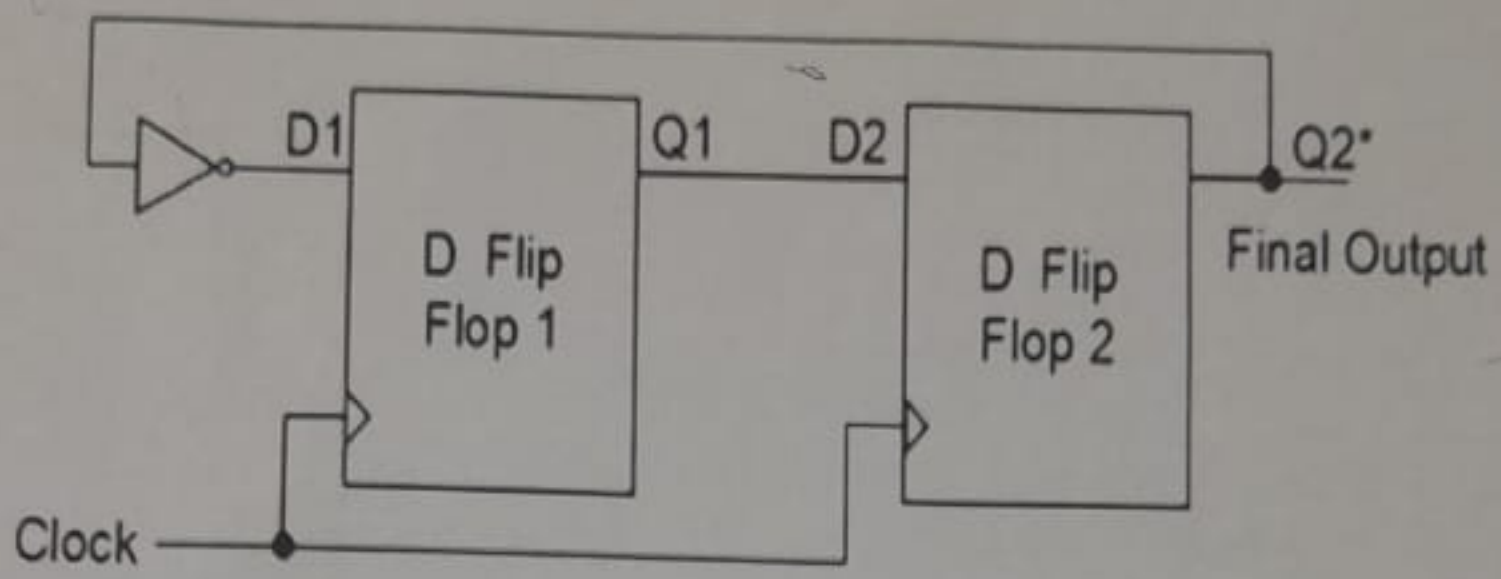
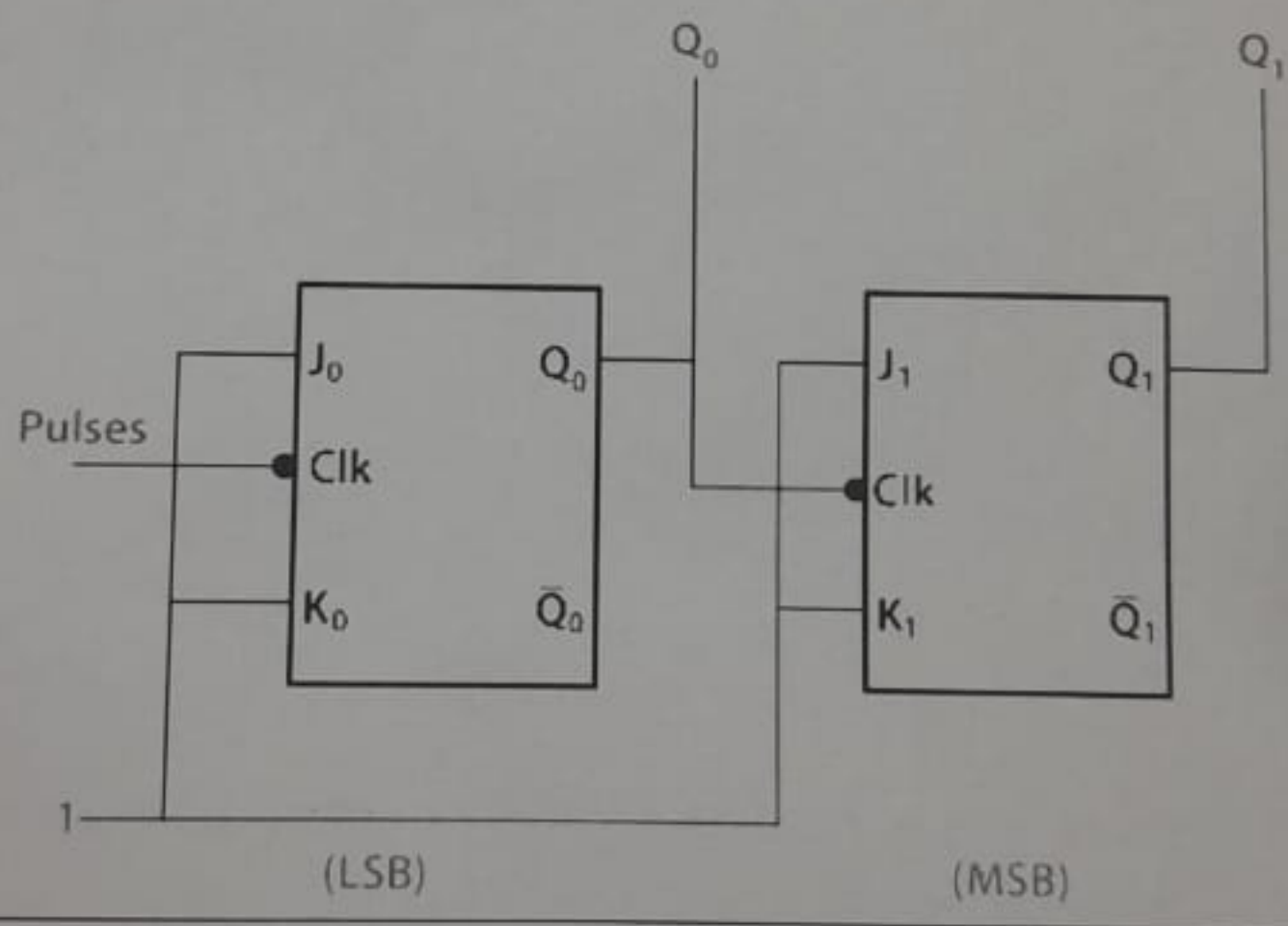
4.	a). Consider the following sequential circuit and the initial value of Q_2 is zero, which means the value of D_1 is one. Draw the waveform for eight clock cycles.	5



	b). Figure below shows the counter and draw the waveform for first 6 pulses of clock pulse input and also the name the counter.	5



5.	Design a sequence detector to detect sequence 1011.	10

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