



SCHOOL OF ELECTRICAL ENGINEERING
WINTER SEMESTER, 2023-24
M.Tech: Integrated course

Class numbers: **VL2023240504493; VL2023240504496; VL2023240504507;**
VL2023240504505;

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CAT- 2

Course Code : **IEEE 102L** Course Title: **Basic Electrical and Electronics Engineering**
Date of Examination : **04.04.2024** Duration : **1 ½ Hours** Maximum Marks : **50**

ANSWER ALL QUESTIONS

(10 × 5 = 50)

- Q1** In a balanced three-phase wye-wye system, the source is an abc-sequence of voltages and $V_{an} = 100\angle 20^\circ$ V rms. The line impedance per phase is $(0.6 + j1.2) \Omega$, while the per phase impedance of the load is $(10 + j14) \Omega$. Calculate all the line currents and line voltages and hence the real and reactive power supplied by the source [10]
- Q2** A staircase light is controlled by two switches, one at the top of the stairs and another at the bottom of stairs. [10]
- Make a truth table for this system
 - Write the logic equation in SOP form
 - Realise the circuit using AND - OR gates
 - Realise the circuit using NAND gates only.
- Q3** Find the minimized expression for implementing the given SOP using Boolean algebra [10]
- $$F(A, B, C, D) = \sum m(3, 7, 11, 12, 13, 14, 15)$$
- Q4** Convert the following numbers. [10]
- $(675.625)_{10} = (?)_{16}$
 - $(10011110)_2 = (?)_8$
 - $(0.BF85)_2 = (?)_8$
 - $(1001.0101)_2 = (?)_{10}$
 - $(0.65625)_{10} = (?)_2$

for 2 given impedances :

$$Z_{eq} = Z_L + Z_{ph}$$

$$I_{ph} = \frac{V_{ph}}{Z_{eq}} \rightarrow I_L \rightarrow V_L$$

$$\cos \phi = (\text{for the load})$$

- Q5** Enumerate the combinational logic circuit k-maps and realise the functions of S_n and C_n and using NAND-NAND to fulfill the condition is shown in Table-1 [10]

Table 1

inputs			output	
A_n	B_n	C_n	S_n	C_n
0	0	0	0 ₀	0 ₀
0	0	1	1 ⁽¹⁾	0 ¹
0	1	0	1 ⁽¹⁾	0 ²
0	1	1	0 ³	1 ⁽³⁾
1	0	0	1 ⁽⁴⁾	0 ⁴
1	0	1	0 ⁵	1 ⁽⁵⁾
1	1	0	0 ⁶	1 ⁽⁶⁾
1	1	1	1 ⁽⁷⁾	1 ⁽⁷⁾