Final Assessment Test – November 2024

VIT Vellore Institute of Technology

Course: ISWE301L - Computer Architecture and Organization
Class NBR(s): 3015/ 3024/3032/3040/3046 Slot: D1+TD1
Time: Three Hours Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions
(10 X 10 = 100 Marks)

1. a) Describe the steps involved in executing the machine instruction. [5]

SUB RO, LOCA

Detailing the transfer between components and the simple control commands required. Assume the instruction is stored at memory location INSTR and the address INSTR is initially held in the PC(Program counter).

b) Write a short note on Multiprocessor and Multicomputer with suitable diagram. [5]

2. a) Consider a 6 GHz CPU in which data processing (arithmetic and logical) instructions take 6 clock cycles for execution and data transfer (load and store) instructions take 10 clock cycles for execution. When a specific program of 2 million instructions run, 60% of the instructions are data processing and 40% of the instructions are data transfer. Calculate the total time taken to run this program. [6]

b) Analyse the status of the condition code flags when the following instruction is executed. [4]

Add R1, R2
where R1=$(EE)_{16}$, R2=$(DF)_{16}$

C
N
V
Z

3. a) Write an Assembly language program to read a line of characters and display it using assembler directives. [5]

b) Describe subroutine linkage and illustrate it with an example that uses a linkage register. [5]

4.(a) Register R1 and R2 of a computer contains the decimal values 4000 and 5600. Base Register BX contains 1500 and index register XR contain 2000. Identify the effective address of the memory operand and also identify the type of addressing modes in each of the following instructions.

i) Load R1, 85 (R2)
ii) Mov #5600, R3
iii) Store 90 (R1, R2), R5
iv) Add (R1) +, R4
v) SUB – (R2), R5
vi) Add 5000, R6
vii) MUL R2, (6000)
viii) INC
ix) Mov R1, [BX] 2400
x) Mov R1,[XR} 2400

4.(b) Write a program to evaluate the arithmetic statement.

$Y = ((C*D) + (E-F) / (G*H))$

- Using a general register computer with three address instructions.
- Using a general register computer with two address instructions.
- Using an accumulator type computer with one address instructions.
- Using a stack organized computer with zero-address operation instructions.

Where C, D, E, F, G, H and Y are memory addresses. In accordance with programming language practice, computing the expression should not change the original value of its operands.

5. You are designing a computer system to handle high-speed data transfer between peripherals and memory without burdening the CPU. Explain the role of the DMA controller in this system.

6.(a) **Design a 512×8 RAM using 128×8 RAM**

i) How many number of RAM chips are required?

ii) How many of these lines are connected to the address input of all chips?

iii) How many lines must be decoded for the chip select input? Specify the size of the decoder.

iv) Draw a memory-address map for the system and give the address range in hexadecimal for RAM.

v) Develop a chip layout for the above said specifications.

OR

6.(b) i) Consider an associative mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find number of bits in tag and tag directory size. **[3]**

ii) Consider a direct mapped main memory size 16GB with block size 4 KB. There are 10 bits in the tag. Find size of cache memory and tag directory size. **[3]**

iii) Consider an 8-way set associative mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find size of main memory and tag directory size. **[4]**

7. a) Perform the arithmetic operations below with binary equivalent in signed Magnitude representation. In each case determine if there is an overflow. Use 5 bits register to accommodate each number. **[3]**

(i) (+10) + (+30) (ii) (-10) + (+30)

b) Perform the arithmetic operations given below with binary numbers and with negative numbers in signed 2's complement representation. Use 7 bits to accommodate each number together with its sign. In each case determine if there is an overflow. **[3]**

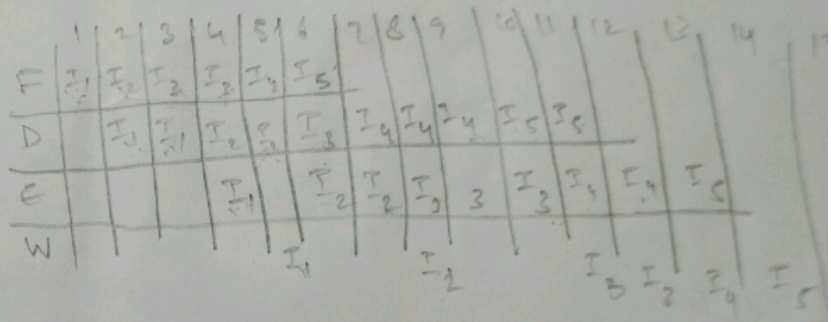
(i) (+35) + (+40) (ii) (−35) + (−40)

c) Derive an algorithm in flowchart form for addition and subtraction of fixed point binary numbers in signed-magnitude representation. **[4]**

8. Perform division for the numbers using restoring division algorithm. Assume the value of Dividend as 53 and the Divisor as 7. Draw the necessary flowchart.

9. a) An instruction pipeline consists of 4 stages Fetch (F), Decode (D), Execute (E) and Write (W). These 5 instructions when executed in a certain sequence need these stages for different number of clock cycles as shown in the table below. **[6]**

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2



Find the number of clock cycles needed to perform all 5 instructions.

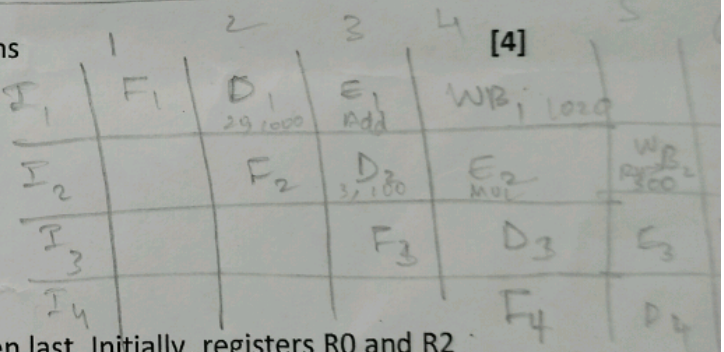
b) Consider the following sequence of instructions **[4]**

i) Add #20,R0,R1

ii) Mul #3,R2,R3

iii) And #$3A,R2,R4

iv) Add R0,R2,R5



In all instructions, the destination operand is given last. Initially, registers R0 and R2 contain 1000 and 100, respectively. These instructions are executed in a computer that has a four-stage pipeline. Assume that the first instruction is fetched in clock cycle 1, and that instruction fetch requires only one clock cycle.

Draw a diagram and describe the operations performed by each pipeline stage during each of clock cycles 1 through 4.

10. a) With neat sketch describe about the structure of general-purpose multiprocessor. **[5]**

b) Illustrate Interconnection networks with suitable example. **[5]**

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