VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act 1956)

REG.NO.:

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT: E1

Programme Name & Branch	:	B.TECH Electronics Engineering (VLSI Design and Technology)
Course Code and Course Name	:	BEVD207L and Computer Architecture
Faculty Name(s)	:	JAYAKRISHNAN P
Class Number(s)	:	VL2024250500780
Date of Examination	:	20/03/2025
Exam Duration	:	90 minutes

Maximum Marks: 50

General instruction(s): Answer All Questions

Q. No	Question	M	CO	BL
1.	A digital computer has a main memory of 128 KB and cache memory of 1 KB with block size of 4 bytes. Determine the address formats in case of a. Direct Mapping b. Associative Mapping c. Set Associative Mapping (four block make a set)	6	3	5
	Consider a computer with 3 levels of memory. Calculate the average memory access time, given the access time and miss rate given below	4		
2.	Consider a CPU with clock cycle of 20ns that executes the program A in 150 clock cycles and access the memory for 100 times during the execution. The CPU uses the cache with miss rate of 5% and Miss Penalty time of 25 machine cycles. Compare the CPU execution time with and without Cache miss.	10	3	5
3.	A computer system uses a virtual address space of 32 bits and a physical address space of 24 bits. The page size is 4 KB. 1. Calculate the number of virtual pages and physical frames. 2. Given a virtual address of 0x12345678, determine the virtual page number and the offset within the page.	4	3	5
	A system has a physical memory consisting of 4 frames. The following sequence of page numbers is referenced by a process: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1	6		

Memory	Access Time(ns)	Miss Rate
Cache (L1)	10	5%
Cache (L2)	20	10%
RAM	60	25%
HDD	100	-

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	Determine the number of page faults using the following page replacement algorithms: 1. First-In, First-Out 2. Least Recently Used 3. Clocking replacement Algorithm			
4.	Represent the given numbers in IEEE 754 Single precision Format (i) -76.19 (ii) 95.62	7	2	4
	(i) Perform the floating-point addition of these two numbers (-76.19 + 95.62) using IEEE 754 rules. Show the intermediate steps, including normalization and rounding	3		
5.	Consider the following code segment, S1: B = M−N; S2: F = A+C; S3: C = A-D; S4: F = A+F; S5: T = X / F; S6: T= X + Y; S7: Y = B + C; S8: C = B+C; S9: B = T +A; S10: N = M+10 i) Determine data dependence and flow dependence between the instructions in the code. ii) Determine the maximum parallelism embedded in this code. iii) Draw the data path for the sequential execution and parallel execution.	10	5	5

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