Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

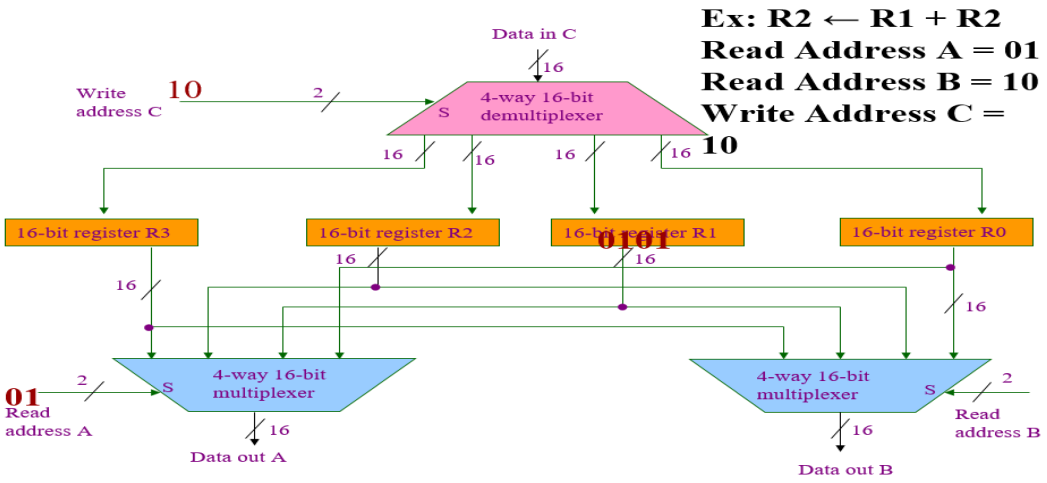
Winter Semester 2024-25
Continuous Assessment Test – I

SLOT: C2+TC2

Programme Name & Branch: B.Tech CSE
Course Name & Code: Computer Architecture and Organization- BCSE205L
Class Number (s): Common to all
Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all five questions

Q. No.	Question	Max Marks
1.	a) Draw the logic diagram of a register file with three access ports and explain the operation of R2 ← R1 + R2 using register files. **Key:** Scheme of Evaluation S.No / Sub Topic / Marks 1 / Logic Diagram / 3 2 / Explanation / 2 **Logic Diagram:**  • Explanation must be given	5

b) Compare and contrast RISC and CISC architectures. Also, Perform C = A+B using RISC and CISC instructions.

5

Scheme of Evaluation

S.No	Sub Topic	Marks
1	Comparison	3
2	Code and explanation	2

Key:

Characteristics of RISC

1.It has simpler instructions and thus simple instruction decoding.

2. More general-purpose registers.

3. The instruction takes one clock cycle in order to get executed.

4.The instruction comes under the size of a single word.

5. Few data types.

6. Simpler addressing modes

7. Pipeline can be easily achieved.

Characteristics of CISC

1. Instructions are complex, and thus it has complex instruction decoding.

2.Lesser general-purpose registers since the operations get performed only in the memory.

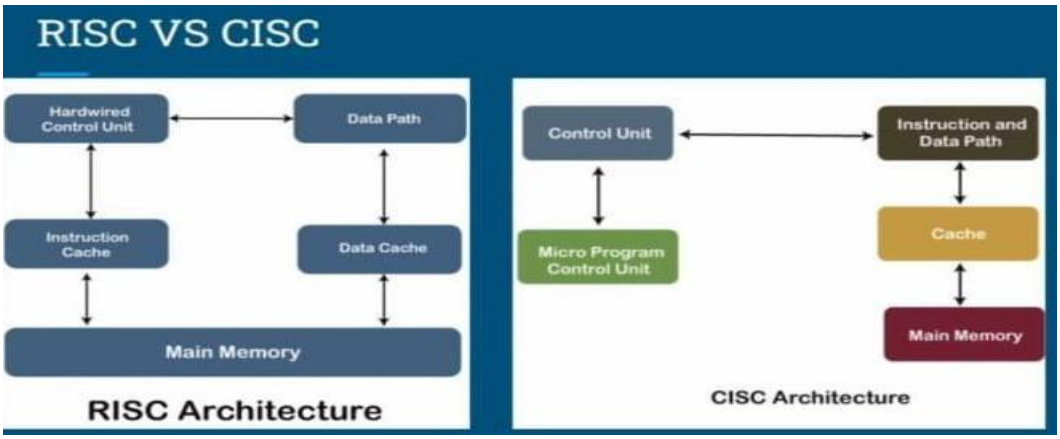
3.The instructions may take more than one clock cycle in order to get executed.

4.The instruction is larger than one-word size.

5. More data types.

6. Complex addressing modes.

7. CISC is not pipelined or less pipeline



C = A + B

CISC operation:

A complex instruction set computer (CISC) is a computer architecture in which single instructions can execute several low-level operations (such as a load from memory, an arithmetic operation, and a memory store). So the CPU has to do more work in a single instruction.

ADD A,B

1. Fetches data from A, fetches data from B, add both and store it in A.

RISC Operation:

A RISC processor executes one action per instruction in one clock cycle.

LOAD A

ADD B

STORE M(X)

- The Load instruction stores the data from a memory location A into accumulator.
- Add operation performs addition on the content of B with accumulator and stores the result in accumulator.
- Finally, store will transfer the accumulator content to the memory location A.

2. Explain the various registers of IAS machine and write the significance of each register. Also demonstrate an assembly code and Register Transfer operation using IAS instructions for the following expression: 10

S = ((U+V)-W)/X

Assume the inputs are available in the memory locations 201 onwards. Store the result in 206 onwards.

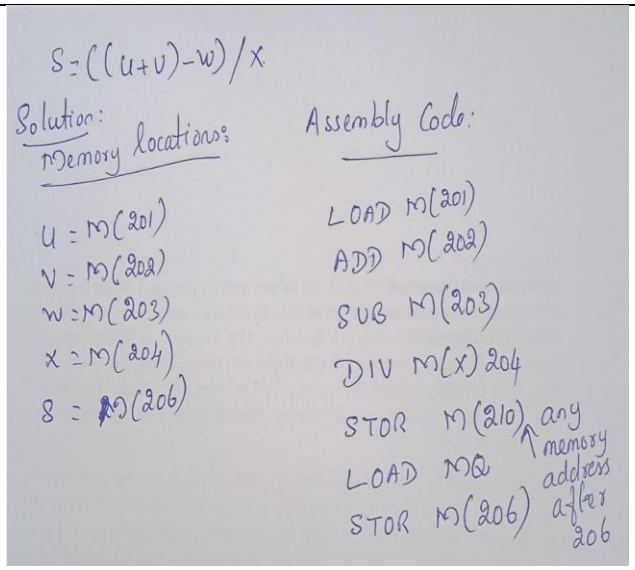
Scheme of Evaluation

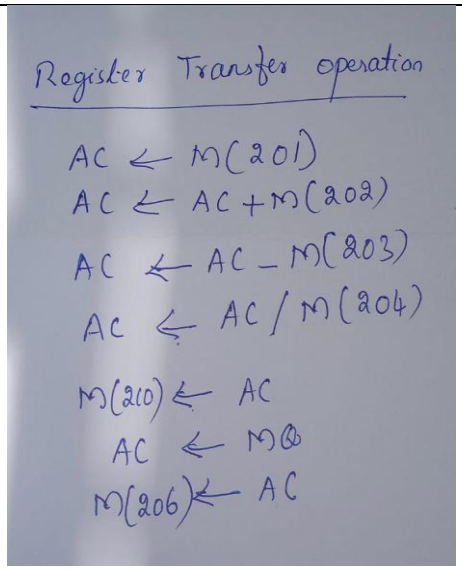
S.No	Sub Topic	Marks
1	Significance of IAS registers	3
2	Assembly code	3
3	Register Transfer operation	4

Solution:

- **Set of registers (storage in CPU)**
  - **Memory Buffer Register (MBR)**
    - Contains a word to be stored in memory or it is used to receive a word from memory or from the I/O unit.
  - **Memory Address Register (MAR)**
    - Specifies the address in memory of the word to be written from or read into the MBR.
  - **Instruction Register (IR)**
    - Contains the 8 bit opcode instruction being executed.
  - **Instruction Buffer Register (IBR)**
    - Employed to hold temporarily the right hand instruction from a word in memory
  - **Program Counter (PC)**
    - Contains the address of the next instruction pair to be fetched from memory
  - **Accumulator (AC) & Multiplier Quotient (MQ)**
    - Employed to hold temporarily the right hand instruction from a word in memory. For eg. The result of multiplying two 40 bit numbers is an 80 bit number, the most significant 40 bits are stored in the AC and the least significant in the MQ.

Assembly code:

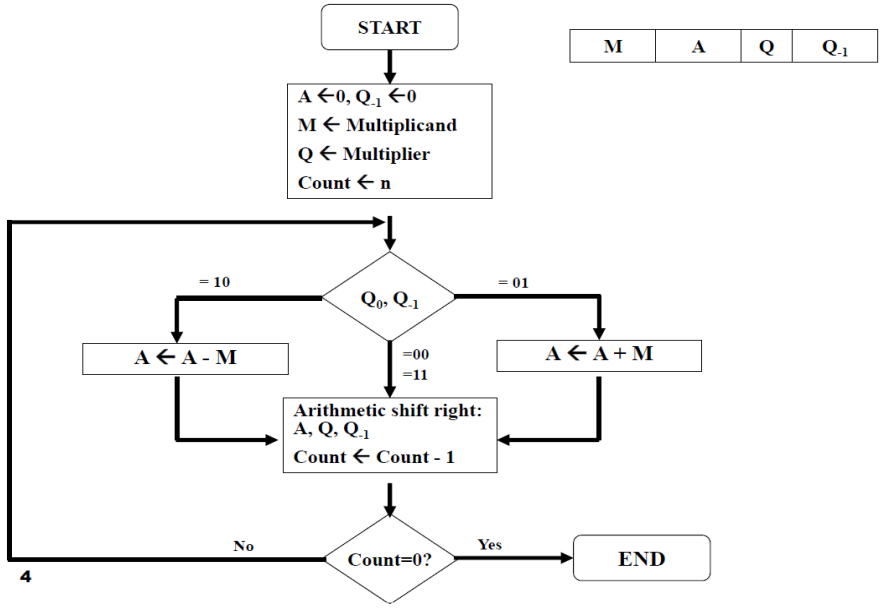




3. a) Illustrate the flowchart of Booth's multiplication algorithm. 4

Scheme of Evaluation

S.No	Sub Topic	Marks
1	Flowchart	4



b) Discuss the Bit Pair recoding table and perform **-20 × 6** using modified Booth's algorithm. 6

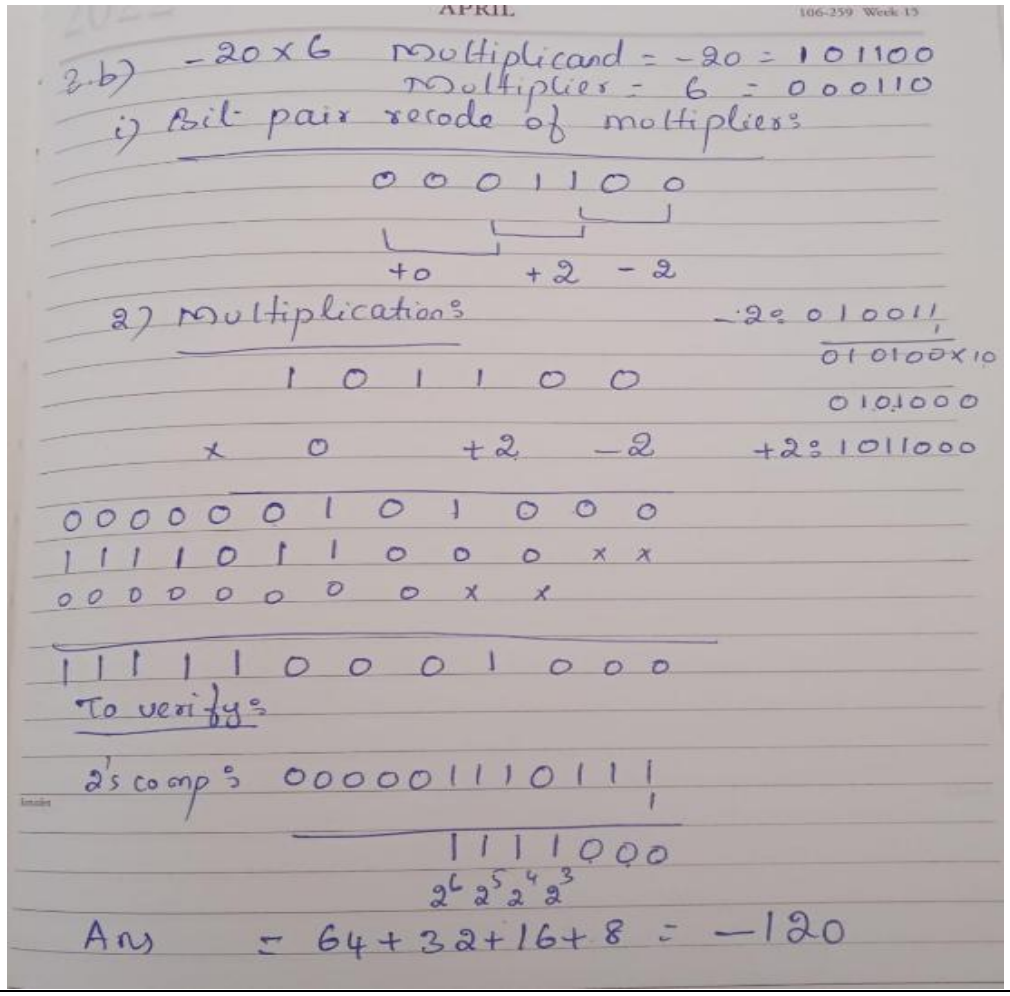
Scheme of Evaluation

S.No	Sub Topic	Marks
1	Recoding Table	2
2	Multiplication	4

Bit Pair recoding table:

i+1	i	i-1	Bit Pair Recode
0	0	0	+0
0	0	1	+1
0	1	0	+1
0	1	1	+2
1	0	0	-2
1	0	1	-1
1	1	0	-1
1	1	1	-0

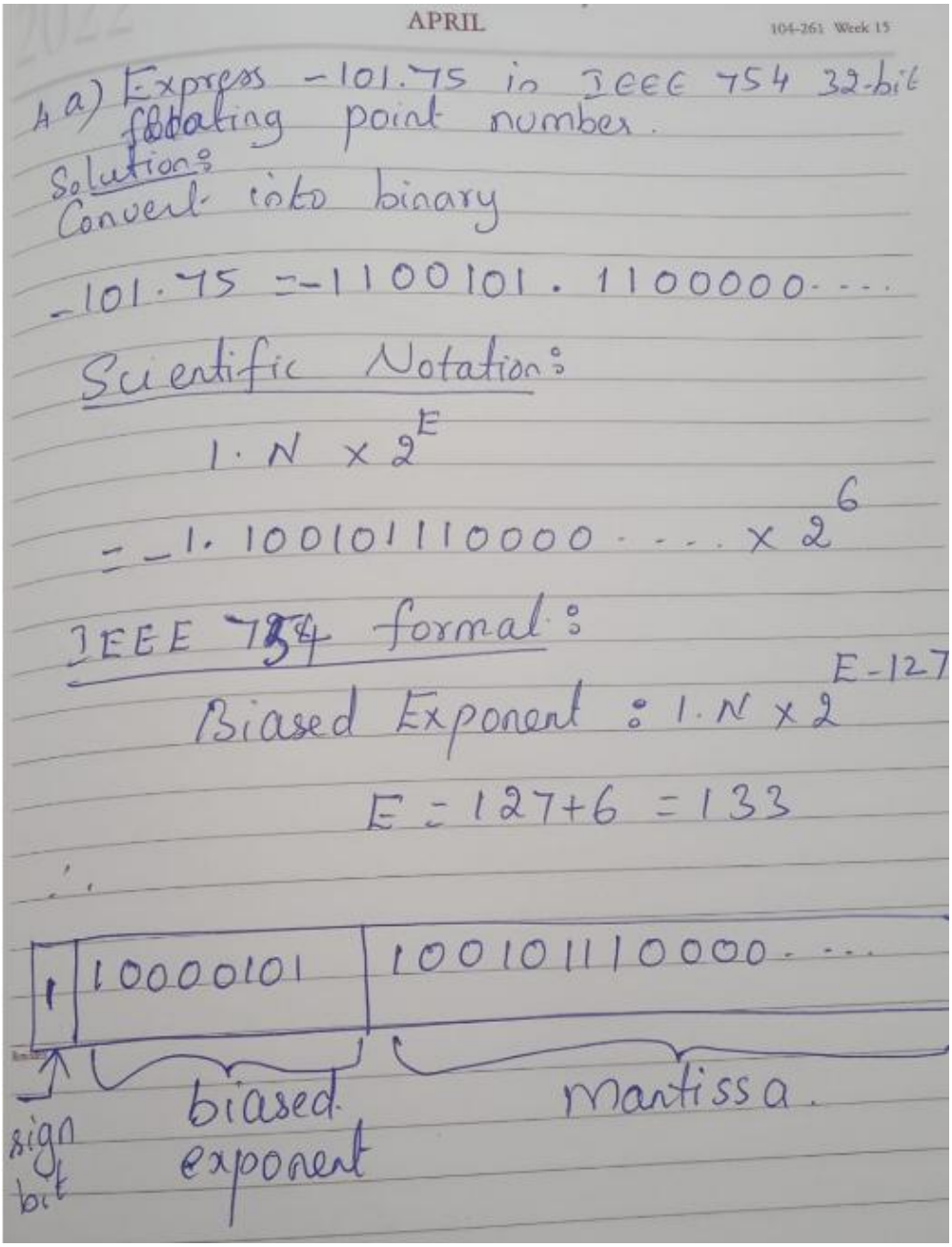
Modified Booth:



4.	a) Express -101.75 in IEEE 754 32-bit floating point number.	5

Scheme of Evaluation

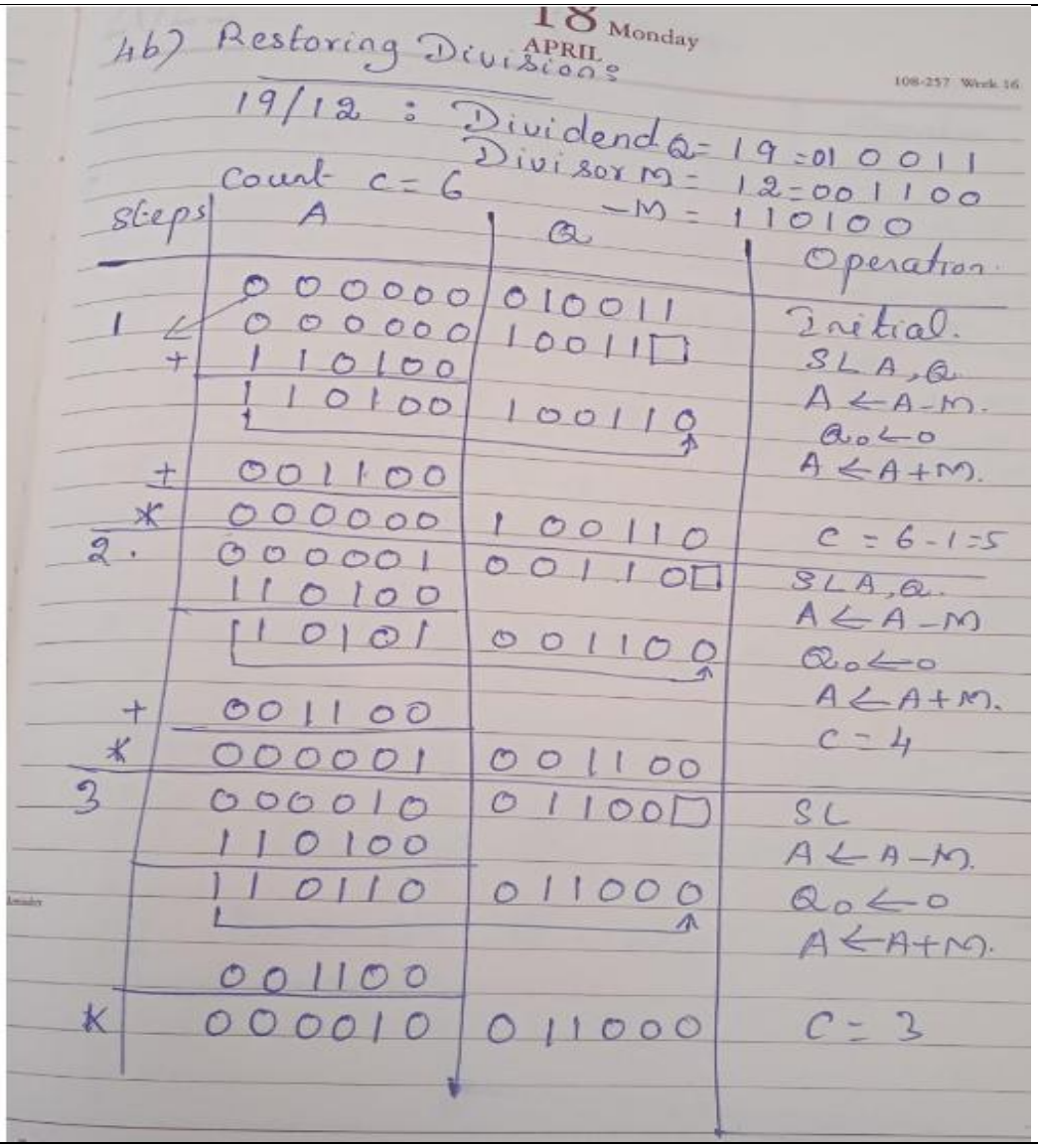
S.No	Sub Topic	Marks
1	Floating point representation	5



b) Perform 19/12 using Restoring division algorithm and describe its operations. 5

Scheme of Evaluation

S.No	Sub Topic	Marks
1	Restoring Division	3
2	Operation description	2



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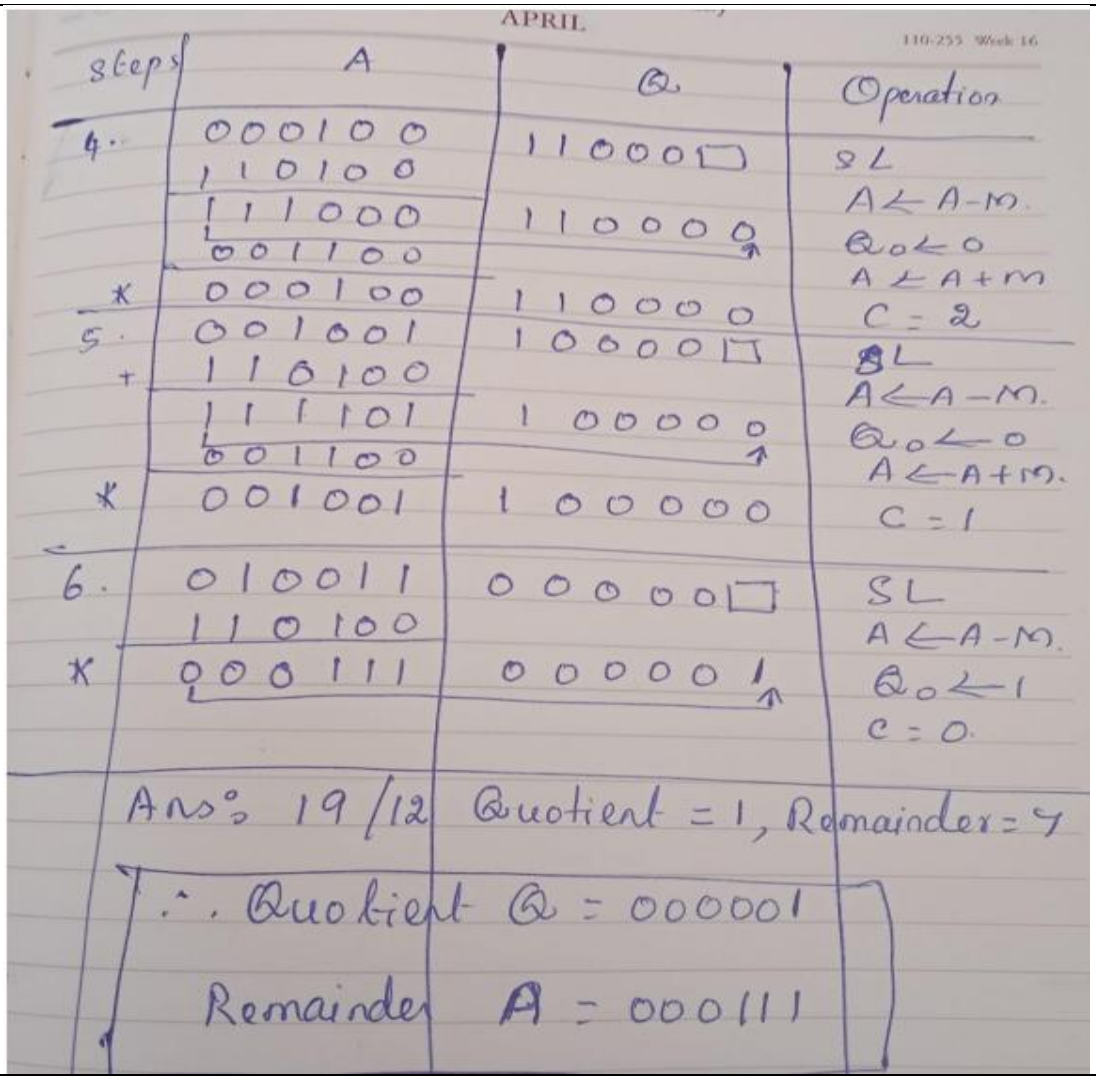
4b) Restoring Division:

19/12 : Dividend Q = 19 = 01 0011
Divisor M = 12 = 001100
−M = 110100
Count c = 6

Steps	A	Q	Operation
	000000	010011	Initial.
1	000000	100111	SL A, Q
+	110100		A ← A−M.
	110100	100110	Q_0 ← 0
+	001100		A ← A+M.
*	000000	100110	c = 6−1 = 5
2.	000001	001100	SL A, Q.
	110100		A ← A−M
	110101	001100	Q_0 ← 0
+	001100		A ← A+M.
*	000001	001100	c = 4
3	000010	011000	SL
	110100		A ← A−M.
	110110	011000	Q_0 ← 0
	001100		A ← A+M.
*	000010	011000	c = 3



5. Map the following categories of instructions to the instructions given below in the prescribed format and justify your answer. 10

S.No	Categories of Instruction	Instruction	Justification
1	Data Movement		
2	Data Processing		
3	Branch		

Instruction Number	Instruction
1	LOAD
2	ADD
3	JUMP

4	SUB
5	LSH
6	RSH
7	MUL
8	STOR
9	MOVE
10	DIV

Scheme of Evaluation

S.No	Sub Topic	Marks
1	Each mapping of instruction carries 0.5 marks (10 X 0.5 =5)	5
2	Justification	5

S.No	Categories of Instruction	Instruction
1	Data Movement	LOAD, STOR, MOVE
2	Data Processing	ADD, SUB, LSH, RSH, MUL, DIV
3	Branch	JUMP

Justification:

i)Data Movement Instructions

LOAD, STOR, MOVE

- LOAD is used to load data from memory to accumulator.
- STORE is used to store the accumulator result in memory.
- MOVE is used to move contents of a register to memory and vice versa or from one register to another

ii) Data Processing Instructions:

ADD, SUB, LSH, RSH, MUL, DIV

- The ADD and SUB instructions are used for performing simple addition/subtraction
- The LSH instruction is used to perform Multiply accumulator by 2.
- RSH instruction is used to perform Divide accumulator by 2.
- The MUL and DIV instructions are used for performing simple Multiplication/Division

iii) Branch Instructions

Jump

- Causes the CPU to jump out of one section of the program into another