



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT:C2+TC2

Programme Name & Branch : B.Tech CSE
Course Code and Course Name : Computer Architecture and Organization- BCSE205L

Q. No	Question	M	CO	BL
1.	Write the assembly code for the given arithmetic statement $W=(X+Y)/Z$ using 0,1,2 and 3 address instructions. Compute memory traffic, memory required to store and encode instructions for 0,1,2 and 3 address machines. Assuming the following fields: addresses - 32 bits, data values -32 bits, opcode - 8 bits and word length - 4 bytes.	10	1	3

	3-address	Memory Access Fetch	Memory Access Execute	Memory Traffic	Memory To Store	Memory To Encode
3-Address	ADD W, X, Y DIV W, W, Z	4 4	3 3	7 7	$4*2=8$ $4*2=8$	$1+(3*2)=7$ $1+(3*2)=7$
Total				14	16 Bytes	14 Bytes
2-Address	MOV W, X ADD W, Y DIV W, Z	3 3 3	2 3 3	5 6 6	$3*2=6$ $3*2=6$ $3*2=6$	$1+(2*2)=5$ $1+(2*2)=5$ $1+(2*2)=5$
Total				17	18 Bytes	15 Bytes
1-Address	LOAD X ADD Y DIV Z STORE W	2 2 2 2	1 1 1 1	3 3 3 3	$2*2=4$ $2*2=4$ $2*2=4$ $2*2=4$	$1+(1*2)=3$ $1+(1*2)=3$ $1+(1*2)=3$ $1+(1*2)=3$
Total				12	16 Bytes	12 Bytes
0-Address	PUSH X PUSH Y ADD PUSH Z DIV POP W	2 2 1 2 1 2	1 1 0 1 0 1	3 3 1 3 1 3	$2*2=4$ $2*2=4$ $2*1=2$ $2*2=4$ $2*1=2$ $2*2=4$	$1+(1*2)=3$ $1+(1*2)=3$ 1 $1+(1*2)=3$ 1 $1+(1*2)=3$
Total				14	20 Bytes	14 bytes

2.	<p>Consider a processor with three instruction classes X, Y and Z, with the corresponding CPI values being 3, 2 and 1 respectively. The processor runs at a clock rate of 2 GHz. For a given program, two compilers produce the following executed instruction counts. Compare the performance of both compilers by computing MIPS and execution time.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th colspan="3">Instruction Count (in millions)</th> </tr> <tr> <th></th> <th>IC_x</th> <th>IC_y</th> <th>IC_z</th> </tr> </thead> <tbody> <tr> <td>Compiler 1</td> <td>4</td> <td>5</td> <td>6</td> </tr> <tr> <td>Compiler 2</td> <td>3</td> <td>7</td> <td>11</td> </tr> </tbody> </table> <p>Answer</p> <p>For compiler 1:</p> $CPI_1 = \frac{4 \times 3 + 5 \times 2 + 6 \times 1}{4+5+6} = 28 / 15 = 1.87$		Instruction Count (in millions)				IC _x	IC _y	IC _z	Compiler 1	4	5	6	Compiler 2	3	7	11	5	1	3
	Instruction Count (in millions)																			
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	$\text{MIPS}_1 = \frac{2000 \text{ MHz}}{1.87} = 1069.52 \text{ MIPS}$ $\text{CPU Execution Time}_1 = \frac{(4+5+6) \times 10^6 \times 1.87}{10^9} = 0.028 \text{ sec}$ <p>For compiler 2:</p> $\text{CPI}_2 = \frac{3 \times 3 + 7 \times 2 + 11 \times 1}{3+7+11} = 34 / 21 = 1.62$ $\text{MIPS}_2 = \frac{2000 \text{ MHz}}{1.62} = 1234.57 \text{ MIPS}$ $\text{CPU Execution Time}_2 = \frac{(3+7+11) \times 10^6 \times 1.62}{10^9} = 0.034 \text{ sec}$																																																																											
	<p>An instruction is stored at location 1000 with its address field at location 1001: the address field has a value of 4000. Address Location 4000 contains 1500. A processor register R1 contains the number 1000 and Index register XR contains the number 200. Evaluate the effective address of the following addressing modes: Direct, Indirect, Relative, Indexed, Register Indirect Addressing Mode.</p> <p>Answer</p> <ul style="list-style-type: none"> • Direct addressing: EA: Address Field = 4000 • Indirect addressing: EA: (Address Field) = (4000) = 1500 • Relative address: EA: PC + Address Field = 1002+4000 = 5002 • Indexed addressing: EA: Address field + Index Register (XR) = 4200 • Register addressing: EA: R1 = 1000 	5																																																																										
3.	<p>A computer employs RAM chips of 1KB and ROM chips of 512 x 8. The computer system needs 1GB of RAM, 4M x 16 of ROM, and two interface units with 256 registers each. A memory mapped I/O configuration is used. The two higher-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.</p> <p>a. Compute the total number of decoders needed for the above system. (4 Marks)</p> <p>b. Design a memory-address map table for the above system. (4 Marks)</p> <p>c. Show the chip layout for the above design. (2 Marks)</p> <p>Answer</p> <table border="1" data-bbox="290 1608 1276 1809"> <thead> <tr> <th>S.NO</th> <th>Memory</th> <th>N x W</th> <th>N¹ x W¹</th> <th>P</th> <th>q</th> <th>p * q</th> <th>x</th> <th>y</th> <th>z</th> <th>Total</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>RAM</td> <td>1KB x 8</td> <td>1GB x 8</td> <td>2²⁰</td> <td>1</td> <td>2²⁰</td> <td>10</td> <td>20</td> <td>2</td> <td>32</td> </tr> <tr> <td>2</td> <td>ROM</td> <td>512 x 8</td> <td>4MBx16</td> <td>2¹³</td> <td>2</td> <td>2¹⁴</td> <td>9</td> <td>14</td> <td>2</td> <td>25</td> </tr> <tr> <td>3</td> <td>Interface</td> <td>256</td> <td>512</td> <td>2</td> <td>1</td> <td>2</td> <td>8</td> <td>1</td> <td>2</td> <td>11</td> </tr> </tbody> </table> <table border="1" data-bbox="290 1841 1189 2027"> <thead> <tr> <th rowspan="2"></th> <th colspan="2">Hex Address</th> <th rowspan="2">31-30</th> <th rowspan="2">29-16</th> <th rowspan="2">16-10</th> <th rowspan="2">9</th> <th rowspan="2">8</th> <th rowspan="2">7-0</th> </tr> <tr> <th>From</th> <th>To</th> </tr> </thead> <tbody> <tr> <td>RAM1</td> <td>00000000</td> <td>000003FF</td> <td>00</td> <td>00..00</td> <td>00..00</td> <td>x</td> <td>x</td> <td>x..x</td> </tr> <tr> <td>RAM2</td> <td>00000200</td> <td>000007FF</td> <td>00</td> <td>00..00</td> <td>00..01</td> <td>x</td> <td>x</td> <td>x..x</td> </tr> </tbody> </table>	S.NO	Memory	N x W	N ¹ x W ¹	P	q	p * q	x	y	z	Total	1	RAM	1KB x 8	1GB x 8	2 ²⁰	1	2 ²⁰	10	20	2	32	2	ROM	512 x 8	4MBx16	2 ¹³	2	2 ¹⁴	9	14	2	25	3	Interface	256	512	2	1	2	8	1	2	11		Hex Address		31-30	29-16	16-10	9	8	7-0	From	To	RAM1	00000000	000003FF	00	00..00	00..00	x	x	x..x	RAM2	00000200	000007FF	00	00..00	00..01	x	x	x..x	10	2 3
S.NO	Memory	N x W	N ¹ x W ¹	P	q	p * q	x	y	z	Total																																																																		
1	RAM	1KB x 8	1GB x 8	2 ²⁰	1	2 ²⁰	10	20	2	32																																																																		
2	ROM	512 x 8	4MBx16	2 ¹³	2	2 ¹⁴	9	14	2	25																																																																		
3	Interface	256	512	2	1	2	8	1	2	11																																																																		
	Hex Address		31-30	29-16	16-10	9	8	7-0																																																																				
	From	To																																																																										
RAM1	00000000	000003FF	00	00..00	00..00	x	x	x..x																																																																				
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RAM2 ⁰	3FFFE00	3FFFFFFF	00	11..11	11..11	x	x	x..x
ROM1.1	40000000	400001FF	01	00..00			x	x..x
ROM1.2	40000000	400001FF	01	00..01			x	x..x
...
Interface1	10000000	100000FF	10	0				x..x
Interface2	50000000	500000FF	10	1				x..x

4.	<p>Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes.</p> <p>a. For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache. (3 Marks)</p> <p>b. Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache. (2 Marks)</p> <p>c. For the main memory addresses of F0010 and CABBE, give the corresponding tag and offset values for a fully associative cache. (2 Marks)</p> <p>d. For the main memory addresses of F0010 and CABBE, give the corresponding tag, cache set, and offset values for a two-way and four-way set-associative cache. (3 Marks)</p> <p>Answer</p> <p>a. Direct Mapping</p> <p>memory addresses: Tag (4 bits) Index(12 bits) Offset(4 bits)</p> <p>F0010 = 1111 0000 0000 0001 0000</p> <ul style="list-style-type: none"> Offset (4 bits) = 0000 = 0 (Hex) Index (12 bits) = 0000 0000 0001 = 1 (Hex) Tag (4 bits) = 1111 = F (Hex) <p>01234 = 0000 0001 0010 0011 0100</p> <ul style="list-style-type: none"> Offset (4 bits) = 0100 Index (12 bits) = 0010 0011 0100 Tag (4 bits) = 0000 <p>CABBE = 1100 1010 1011 1011 1110</p> <ul style="list-style-type: none"> Offset (4 bits) = 1110 Index (12 bits) = 1010 1011 1011 	2	3
		10	



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	<ul style="list-style-type: none"> • Tag (4 bits) = 1100 <p>b.</p> <p>01234 = 0000 0001 0010 0011 0100 Index = 0x234 Tag = 0</p> <p>81234 = 1000 0001 0010 0011 0100 Index = 0x234 Tag = 8</p> <p>c. Fully Associative Cache</p> <p>F0010 Tag = 1111 0000 0000 0001 Offset = 0000 (0)</p> <p>CABBE Tag = 1100 1010 1011 1011 Offset = 1110 (E)</p> <p>d. Set-associative</p> <p>2-way addressing: Tag (5 bits) Index(11 bits) Offset(4 bits) 4-way addressing: Tag (6 bits) Index(10 bits) Offset(4 bits)</p> <p>F0010: 1111 0000 0000 0001 0000</p> <p>2-Way: Tag = 11110 Set Index = 0000 0000 000 Offset = 0000</p> <p>4-Way: Tag = 111100 Set Index = 0000 0000 00 Offset = 0000</p> <p>CABBE:1100 1010 1011 1011 1110</p> <p>2-Way: Tag = 11001 Set Index = 0101 0111 011 Offset = 1110</p> <p>4-Way: Tag = 110010 Set Index = 1010 1011 10 Offset = 1110</p>			
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5.	<p>Explain how I/O Controller manages communication between the CPU and peripheral devices in detail with neat diagrams.</p> <p>Answer</p> <p>An I/O Controller is a specialized hardware component that acts as a bridge between the CPU, memory, and peripheral devices (such as printers, keyboards,</p>		3	2
		4		



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<p>hard drives, and network interfaces). It manages communication, controls data transfers, and offloads processing from the CPU.</p> <p>The I/O Controller performs several key functions:</p> <ul style="list-style-type: none"> • Interface Management: Connects peripheral devices to the CPU. • Data Transfer Control: Manages the movement of data between memory and I/O devices. • Synchronization: Ensures that slow peripheral devices do not affect CPU performance. • Interrupt Handling: Sends interrupts to the CPU when a device is ready. • Error Detection & Correction: Ensures reliable data transmission. <p>The I/O Controller manages communication between the CPU and peripheral devices in a step-by-step manner:</p> <p>Step 1: CPU Sends a Command The CPU sends a request (Read/Write) to the I/O Controller via the System Bus. The command includes: Device Address (to specify which device to communicate with). Operation Type (Read or Write). Memory Address (where to store or retrieve data).</p> <p>Step 2: I/O Controller Communicates with the Device The I/O Controller decodes the CPU's command. It checks the status register to see if the device is ready. If the device is busy, the controller waits until it is free.</p> <p>Step 3: Data Transfer Once the device is ready, the I/O Controller transfers data between the device and memory. This transfer occurs using one of the following methods: Programmed I/O: CPU continuously monitors the device. Interrupt-Driven I/O: Device sends an interrupt signal when data is ready. Direct Memory Access (DMA): Data is transferred directly between memory and the device without CPU intervention.</p> <p>Step 4: Interrupt Handling</p>			
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