Final Assessment Test – May 2024

VIT
Vellore Institute of Technology

Course: BCSE205L - Computer Architecture and Organization
Class NBR(s): 0777/0786/0792/0802/0805/0811/0818 /0836/0848/0853/0862/0870/0878/0883/0885/0892 /0898/0900/0905/0907/0910/0916/1071 Slot: D2+TD2
Time: Three Hours Max. Marks: 100

- KEEPING MOBILE PHONE/ELECTRONIC DEVICES EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer any TEN Questions

(10 X 10 = 100 Marks)

1. a) Explain about the Registers and Register file. [4]

   b) Write an assembly code for computing M=(N-P)*Q expression using IAS instructions [6]

   Assume that inputs are available in the memory locations 601 and 602,603. Store the result in memory locations 604 and 605.

2. a) Multiply the following pair of signed numbers -9*-13 using modified Booth Algorithm [6]

   b) Describe the IEEE representation of floating point numbers and represent 85.125 in single precision format. [4]

3. List out the Boolean expressions for control signals for an example instruction execution and investigate the components required for hardwired control logic. Design the Hardwired based control unit.

4. a) Our favourite program runs in 12 seconds on computer A, which has a 4GHz clock. We are trying to help a computer designer build a computer, Which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.5 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? [5]

   b) Write the code to implement the expression A= (B-C)*D on 3 address and 2 address machines. Do not rearrange the expression. In accordance with programming language practice, computing expression should not change the values of its operands. And also compute the total memory traffic in bytes for both instruction fetch and instruction execution for code and implement the expression evaluation for the above said two machines. Assume that opcode occupy one byte, address occupies two bytes, data values occupy two bytes and word length one byte. [5]

5. A computer employs RAM chips of 128 x 8 and ROM chips of 512 x 8. The computer system needs 256 x 16 of RAM, 1024 x 16 of ROM, and two interface units with 256 registers each.

   a) Compute total number of decoders are needed for the above system?
   b) Design a memory-address map for the above system
   c) Show the chip layout for the above design with a neat sketch.

6. a) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit words. [6]

   i. How many bits are required for addressing the main memory?

   ii. How many bits are needed to represent the TAG, SET and WORD fields?

   b) Assume that a computer system employs a cache with an access time of 20ns and a main memory with a cycle time of 200ns. Suppose that the hit ratio for reads is 90%. [4]

   i. What would be the average access time for reads if the cache is a "look-through" cache?

   ii. What would be the average access time for reads if the cache is a "look-Aside" cache?

7. Draw the typical block diagram of a DMA controller and explain the various transfer modes that are used for direct data transfer between memory and peripherals.

8. Discuss various bus arbitrations methods followed to handle the priority request with the necessary diagrams.

9. a) Consider the input data to be transmitted is 1011010, Construct the encoded data using the hamming code method. [5]

   b) Assume the data received is 10100010000 which contains an error, identify the error bit position and correct the bit using hamming error correction and detection technique. [5]

10. Discuss in details, The RAID levels. Will RAID level increase the performance? Justify in details.

11. Explain data hazard and the ways to detect and handle the data hazards in the below mentioned sequences.

```
sub $2, $1,$3
and $12,$2,$5
or $13,$6,$2
add $14,$2,$2
sw $15,100($2)
```

12. a) Consider the execution of a program which results in the execution of 2 million instructions on a 500-MHz processor. The instruction mix and the CPI for each instruction type are given in below the table. [5]

Compute MIPS (Million Instructions Per Second) Rating using given data.

Instruction type	CPI	Instruction Mix
Arithmetic and Logic	1	60%
Load/Stored with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

   b) Suppose you want to achieve a speed-up of 90 times faster with 100 processors. What percentage of the original computation can be sequential? [5]

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