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VIT
Vellore Institute of Technology

School of Computer Science Engineering and Information Systems

Fall Semester 2024-2025

Continuous Assessment Test – I

Programme Name & Branch : B.Sc (CS)
Course Name & code: Computer Organization and Architecture & UCSC103L
Class Number (s): VL2024250103021
Faculty Name (s): Dr. Vanitha M
Exam Duration: 90 Min.
Maximum Marks: 50

Answer ALL Questions

Q.No.	Question	Max Marks
1.a	Conversion of decimal number **10.625** into binary number	3
b.	Subtract **(+80) and (-70)** using 2's complement	3
c.	Obtain the 1's and 2's complement of the following binary numbers **1010101 ,0111000 , 0000001 , 10000 , 00000**	4
2.	Discuss in detail, the working of Full Adder logic circuit and extend your discussion to explain a binary adder, which can be used to add two binary numbers.	10
3. a.	Reduce the following equation using k-map $F(a,b,c)=\sum m(1,2,3,4,5)$	5
b.	Design the SR flip-flop using NOR gate	5
4.	A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations i. A is False, B is True, C is True ii. A is False, B is True ,C is False iii. A, B, C are False iv. A, B, C are True Write the Truth table for F. Use the convention True=1 and False = 0. a) Write the simplified expression for F in SOP form. b) Draw logic circuit using minimum number of 2-input NAND gates	10
5.a.	Write short notes on the following : (i)Data transfer instructions (ii) Data manipulation instructions	5
b.	Explain the phases involved in Instruction cycle.	5