REG.NO [redacted]

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Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2024-2025

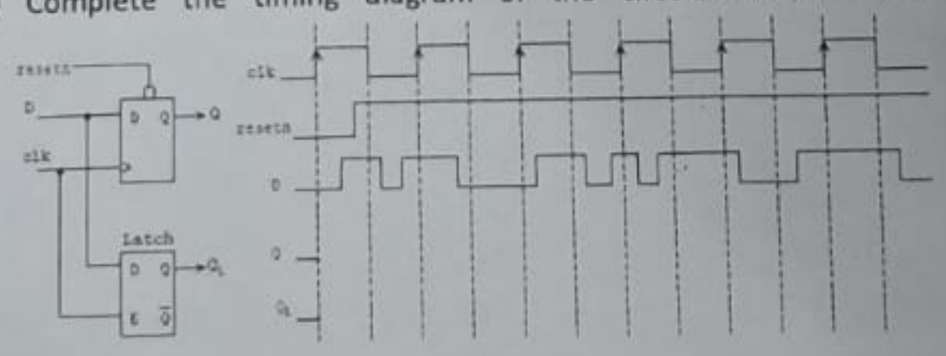
SLOT: B1+TB1

Programme Name & Branch	**:B.Tech. (EEE,EIE)**
Course Code and Course Name	: BEEE206L - Digital Electronics
Faculty Name(s)	: Prof. R. Santhakumar / Prof. S. Balamurugan
Class Number(s)	: VL2024250101246 / VL2024250101245
Date of Examination	: 14 Oct. 2024
Exam Duration	: **90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)

1. Develop digital logic circuits and apply to solve real world applications.
2. Design and analyze digital circuits using Verilog HDL.
3. Design and implement combinational circuits, sequential circuits and programmable logic devices.

Q. No	Question	M	CO	BL
1.	Design and Write Verilog code for BCD to seven segment display using structural modelling.	5+5	1	BL3
2.	a) Convert SR flip-flop JK flip-flop and write Verilog code for the JK flip-flop circuit using behavioral modelling.	6+4	2	BL2
	b) Complete the timing diagram of the circuits shown below 			
3.	Design synchronous sequential circuit using D flip-flop for the following state diagram.	10	3	BL2

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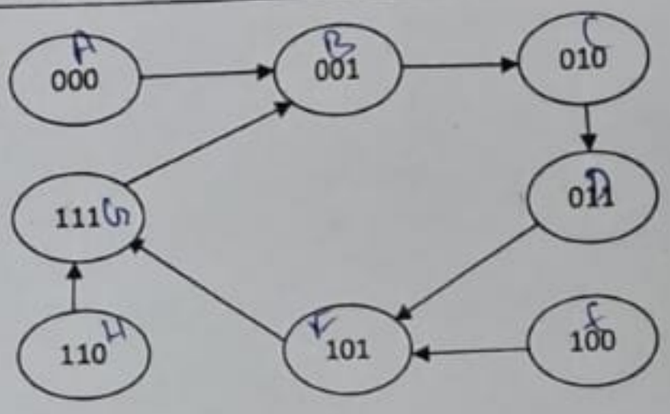

4.	Design a sequence detector to detect sequence 1101 from input sequence x using Mealy machine overlapping method. Implement the circuit using T flip-flop.	10	3	BL4

5.	a) From the following code
	
	assume a = 5; assume b = 8; assume c = 13;
	assume w = 5; assume x = 8; assume y = 13;
	
	initial begin
	a = b + c;
	b = c + a;
	c = a + b;
	end
	initial begin
	w <= x + y;
	x <= y + w;
	y <= w + x;
	end
	
	Write the values stored in a,b,c,w,x,and y after exaction of the above code.
		4+6	2	BL4

	b) Write the Verilog code to implement 3:8 decoders using 2:4 decoders.			